ANALOG SIGNAL PROCESSING TECHNIQUE: THE CURRENT-MODE APPROACH

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ABSTRACT

This paper presents the design of an A/D converter. The objective of this research is to determine whether a discrete-time approach is the best choice for incorporating the A/D converter into a silicon fully-integrated Hearing-Aid system. In that sense, power consumption, conversion time, and integration area were basic parameters for designing a test chip, which was fabricated and tested. First experimental results are presented.

RESUMEN

En este artículo se presenta el diseño de un convertidor A/D. El propósito de esta investigación es determinar si una aproximación en tiempo discreto convertidor es la mejor opción para incorporar el convertidor A/D en un dispositivo de ayuda auditiva completamente integrada en silicio. En este sentido, parámetros básicos como consumo de potencia, tiempo de conversión y área de integración fueron tomados en consideración para el diseño de un chip de prueba, el cual fue fabricado y caracterizado. Se presentan los primeros resultados experimentales del convertidor.

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ABSTRACT

This paper presents the design of an A/D converter. The objective of this research is to determine whether a discrete-time approach is the best choice for incorporating the A/D converter into a silicon fully-integrated Hearing-Aid system. In that sense, power consumption, conversion time, and integration area were basic parameters for designing a test chip, which was fabricated and tested. First experimental results are presented.

1. INTRODUCTION

The design of a Hearing-Aid device is a multi-disciplinary work. When the input transducer is fabricated with electronics for signal processing, it is basic to have control of both the mechanical properties of the CMOS materials and knowledge of the required analog/digital circuits. The first requirement assumes that the etching/patterning process to be applied constitutes an integral part of a well-established surface/bulk micromachining technique. While the last one, in order to obtain the correct electrical response, is focused on suitable signal processing techniques. Hence, this research takes into account the development of a fully integrated hearing-aid device in which the purpose is to integrate also the input transducer, mainly a microphone, and the electronics to amplify just the required signals to suitable sound levels. A description of a Hearing-Aid device is depicted in Fig. 1a. The input transducer induces a band-limited characteristic because of its geometrical size produces a dominant pole; however, the pole's position is generally under the designer's control (the simplest approach for modeling the microphone is shown in Fig. 1b). A preamplifier circuit is responsible for processing the signal provided by the transducer and its response must be as much as possible noiseless. The analog signal is then passed to the A/D converter and, just in that step, the hearing impairment can be compensated using the medical hearing-data that were previously incorporated to the programmable filter. After that, a D/A converter and a power circuit are needed to produce a suitable sound level. Thus, for designing a Hearing-Aid device it is basic to have knowledge of both fabrication processes and techniques for designing analog/digital circuits.

According the description given above this paper describes just the design of an A/D converter, while details of both modeling and fabrication of the input transducer can be found in [1]-[3]. In section 2 of this paper, the basics for designing the A/D converter are presented. Section 3 discusses the experimental results. The data were obtained of a test chip, which has been developed in a 1.2μm CMOS fabrication process. At the end of the paper some conclusions are given.

2. THE A/D CONVERTER

This circuit is a basic system for processing the signal provided by a previous circuit. A common technique for designing such a system is the named switched-current $\Sigma\Delta$ converter [4]. The advantage of such a technique is not only that it can be implemented in CMOS digital technologies but also that the basic building block is the current mirror (CM). The latter requires low bias voltage for its operation as well as minimum integration area. In practice, switched-current (SI) suffers of several non-idealities because of the switching process, however, in order to minimize them we have used the compensation technique reported in [5].

A. Basics on $\Sigma\Delta$

There are four needed steps to perform an analog-to-digital conversion:

1) <u>Antialias filtering</u> to prevent folding into the baseband during the sampling process;

2) When <u>sampling</u> is applied to a continuos-time signal x(t) , the frequency $\mathbf{f_s}$ produces a sequence x(nT) , where the sampling period $\mathbf{T}$ is given by 1/$\mathbf{f_s}$, here $\mathbf{n}$ is an integer;

3) During <u>quantization</u> each sampled continuos-amplitude signal corresponds to a signal that is discrete in time and amplitude;

4) In the <u>encoding</u> step each discrete value supplying a digital signal just at the output of the ADC.
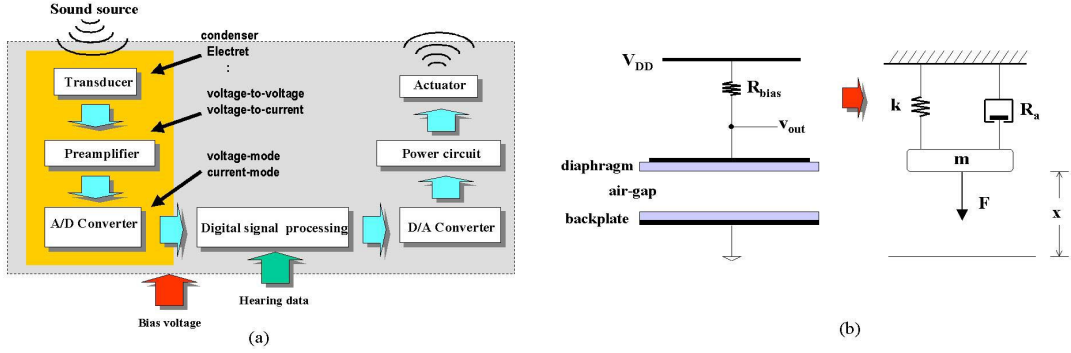
Fi**g. 1** A simple description of a Hearing-Aid device (a). A parallel-plate microphone can be described by a mechanical model (b). In practice, the diaphragm deformation is represented with one generalized displacement coordinate, **x**.

When sampling $\mathbf{f_s}$ exceeds the Nyquist rate ($\mathbf{f_N}$) the oversampling ratio is given by $\mathbf{M=f_s/f_M}$. As a consequence, when the input signal is oversampled its corresponding band-limited spectrum is shifted upward a frequency given by $\mathbf{Mf_N}$, therefore the anti- alias filtering is not yet a needed requirement. From the analog IC designer's point of view this fact means an important reduction of both integration area and power consumption.

B. Description of the ΣΔ modulator

The basic structure discussed here is a Low-Pass Second-Order ΣΔ modulator illustrated in Fig. 2. It consists of two integrators, a quantizer, as well as two 1-bit Digital-to Analog converters (DAC). By looking at the structure we know that SI circuits can be used for substituting each depicted block. Using this approach, the memory cell will be the basic building block. As it is well known the memory cell must be based in a cascode current branch with added switches [5]. Such an array compensates in its entirely the majority of the switching process non-idealities (see Fig. 3). This fact is a fundamental characteristic of it because reducing its non-idealities the ΣΔ modulator increases its performance.

The current integrator is obtained once a unitary feedback loop is applied to the full-delay circuit that is obtained by cascading simply two memory cells. As far as this circuit is feedback connected the resulting integrator presents a redundant parallel switch connection since each one operate with complementary clocking scheme (Φ_2 and Φ_2). Furthermore, a continuos-time output current branch must be included to measure the current integrator response. In this work the integrator was designed for obtaining a modulator gain of $\mathbf{a}$=½.

C. Signal-to-Noise Ratio Analysis

It is known that the signal-to-Noise ratio (SNR) for an **N**-th order ΣΔ modulator is given by

$$SNR = \frac{3}{2} \cdot \frac{2N+1}{\pi^{2N}} \cdot M^{2N+1} \qquad (1)$$

which is defined as the ratio of the power of a full-scale sinusoidal signal to the in-band quantization noise power. Here (1) assumes that the quantization error is considered as white noise having equal probability of laying on the range $\pm\Delta/2$, where Δ is the quantization step size. Assuming that $\mathbf{M}=2^r$, where **r** is the doubling factor of the oversampling ratio, it can be substituted into (1) to express SNR as function of the number of bits

$$SNR\big|_{N=2} \approx 2.5r - 2 \qquad (2)$$

hence the SNR increases for high values of **r**. Taken into account the entire audio frequency range, the digital word length can be from 12bits up to 14bits (equivalently 72-84dB). Therefore, by applying (2) the deduced rounded-off doubling-factor is r=7.
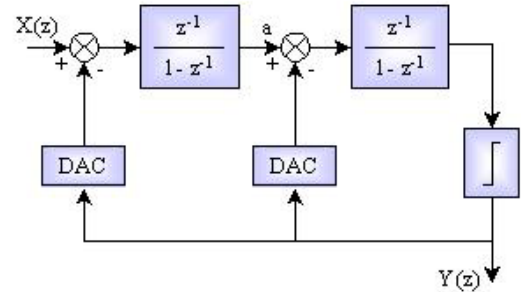
Fig. 2 ΣΔ modulator. A second order design is recommended because the quantization noise is not correlated.
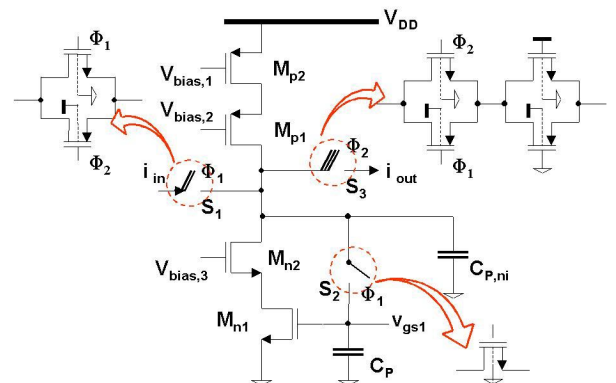
Fig. 3 The half-delay cell. In this work all switches have minimum size (1.8μm/1.8μm). Here $C_P=C_{gs}$.

D. Power Noise

This non-ideality is the main one in the integrator, thus, reducing the power noise ($\mathbf{P_{n1}}$) of the input integrator (see Fig. 2) the overall **SNR** of the modulator will be enhanced. There are several ways for reducing $\mathbf{P_{n1}}$:

- Increasing the capacitance C_{gs} of the memory transistor M_{n1}, and/or

- Using a high oversampling ratio **M**.

In practice C_{gs} has to be necessarily increased because of the settling-time requirement. As a consequence, the resulting purpose of the high size for C_{gs} is twofold. On the other hand, as the modulator was designed in order to operate in a bandwidth of 20 kHz, **M** was 128 since r=7. According to these design considerations, we expect a real reduction for $\mathbf{P_{n1}}$.

E. Switched-Current Design

The quantizer has been implemented by means of a high-speed current comparator and the 1-bit DAC was simply designed using current sources controlled by the modulator's output. By assuming a sinusoidal input current (full-scale power of $\Delta^2/8$) the SNR of the Low-Pass Second-Order $\Sigma\Delta$ modulator can be approximated by

$$SNR = 10\log\left(15M\left(2\left(\frac{\pi}{M}\right)^4 + 640 m_{th}kT\frac{1+\frac{g_{mn}}{g_{mp}}}{C_{gs1}(V_{gs}-V_{tn})^2_{M1}}\right)^{-1}\right) \quad (3)$$

where $(V_{gs}-V_{tn})^2_{M1}$ is the first order approximation of the saturation voltage of memory transistor M_{n1}, $\mathbf{m_{th}}$ is a constant of the fabrication process between 1 and 2.5, $\mathbf{k}$ is the Boltzmann constant, $\mathbf{T}$ is the absolute temperature. Equation (3) shows how important is the C_{gs} value. As was mentioned before, a high value of it not only increases the SNR of the $\Sigma\Delta$ modulator but also reduces the magnitude of glitches due clocking [6]. Actually, the capacitance C_{gs} has a value of 1.0pF and it is a MOS transistor (W/L=131.4μm/6.0μm) with its drain and source shortened to V_{SS}. Additionally, (3) considers the following assumptions

- The second integrator contributes only marginally to the total noise of the modulator.

- The voltages for biasing the current branches are stable voltage sources.

Using the design directions given by (3), it is simple to size the current integrator in order to reach both a bandwidth of 20kHz for the modulator and the needed resolution.

When this design is compared with a voltage-mode approach [8], there are several advantages to postulate that SI is the correct choice for designing a A/D converter.

3. EXPERIMENTAL RESULTS

The 2nd order $\Sigma\Delta$ modulator occupies 0.25×0.17mm² without bonding pads and it was implemented in a 1.2μm N-well CMOS technology. The test chip also includes an internal clock generator and additional digital circuitry. The latter is for analyzing the generation of digital noise, which will be described in a future paper.

The input signal frequency was 10kHz and the modulator output pulses were stored and then a 2048 points FFT was applied. This procedure is useful to determine the power spectral density (PSD). After that, the SNR plus Distortion ratio was measured by dividing the power of the signal between the power of noise (obtained from PSD) in the 20kHz bandwidth. As Fig. 4 shows the maximum value of SNRD from simulations is 80dB, while the corresponding data for measurements is 66dB. According this result an 11-bit digital word length can be obtained, which corresponds to one bit least that the minimum number of bits for processing audio signals.

The measurement modulator output spectrum for a sinusoidal input signal of -9dB input level and 10kHz frequency shown spikes-less out-of-band. That result suggests that the quantization error is certainly white noise, however, the constant noise floor in the baseband was slightly higher than expected.

In order to express the SNR as function of the resulting number of bits, we propose the following model

$$SNR\big|_{N=2} \approx 2.5r - (2+\alpha) \quad (4)$$

where α represents the lost bits and it could be due the following:

- Digital switching noise that is added to sensitive nodes via the MOS Capacitor, C_{gs},

- The distortion components affect the behavior of the modulator as the input signal is increased. This is the case mainly of C_{gs},

- The $\Sigma\Delta$ modulator is sensitive to the non-idealities of the DAC in the main feedback loop, since the resulting error is directly added to the input.

- The PCB, in which the chip was attached, is a candidate for been considered a source of non-idealities because it was not optimized for noise reduction.
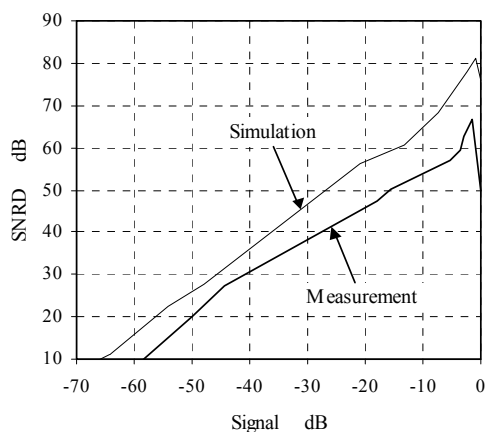
Fig. 4 The SNRD comparison result. The discrepancy is attributed to factors that were considered negligible in the process design.

4. CONCLUSIONS

In this paper the design and experimental results of a 2nd order $\Sigma\Delta$ modulator have been presented. The deduced resolution was 2 bit short of the one specified. Several factors are the reason why the design does not satisfy the original specifications. However, we can conclude that our design with tiny modifications allow us to reach more than the minimum number of bits for processing audio signals. Currently the modulator is being redesigned to minimized second order effects and, in a future paper, we will describe the procedure for minimizing α and obtain at least a 12-bit A/D converter.

Finally, up to now the experimental results indicate that a 2nd order $\Sigma\Delta$ A/D converter may be used in those applications in which magnetic field detection are needed [7]. Certainly that is a different field application respect the described one at the beginning of this paper, however, for increasing the duty-cycle of batteries (a hearing aid is a wire-less device) a MAGFET as well as integrated inductors are required devices in this research.

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