A SIMPLE MODEL FOR A NEW SOI MOSFET WITH ASYMMETRIC TRAPEZOIDAL GATE

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ABSTRACT

The Asymmetric Trapezoidal Gate (ATG) MOSFET has a narrow drain-side width as compared to the source side, what leads to a small drain-junction capacitance with higher drain current capacity than an equivalent rectangular gate device. This characteristic, besides the scaling down and Silicon on Insulator (SOI) structure adoption, benefits the improvement in speed. This work will focus on a simple current model for a thin-film, fully depleted SOI device. The model can also be applied to edgeless MOSFETs, that can be considered as a composition of four ATGs. It's defined a shape current gain, as the ratio between the trapezoidal-gate device current and a rectangular-gate device with the same drain width. The output of Da Vinci 3D simulator is used as a reference for model validation. In triode operation region the error ranges from 0.5 to 6.5% for simulated devices. In saturation region, error is even smaller.

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1. INTRODUCTION

The scaling-down of MOS devices benefits the improvement in speed, because it results in decrease of drain, gate, and overlap capacitance. For submicron devices the reduced gate length results in small intrinsic gate capacitance and then the dominating factor on speed performance becomes drain junction parasitic capacitance, at the transistor level. The Asymmetric Trapezoidal Gate (ATG) MOSFET has a narrow drain-side width, as compared to the source side, as shown in Figure 1, what leads to a small drain-junction capacitance with higher drain current capacity than an equivalent traditional rectangular-gate device. Some models for bulk technology ATGs with different degrees of complexity and precision were developed [1], [2]. The advantages offered by ATG in bulk technologies can be expanded greatly by migrating to Silicon on Insulator(SOI) technology. This work will focus on a simple current model for a thin-film, fully depleted SOI device. Such model will be derived based on gradual-channel approximation (GCA) and charge sheet assumption. A first current-voltage function is derived for triode region and a shape-dependent current factor K_W is defined. Some simulation results show that the same factor may be applied to saturation region.

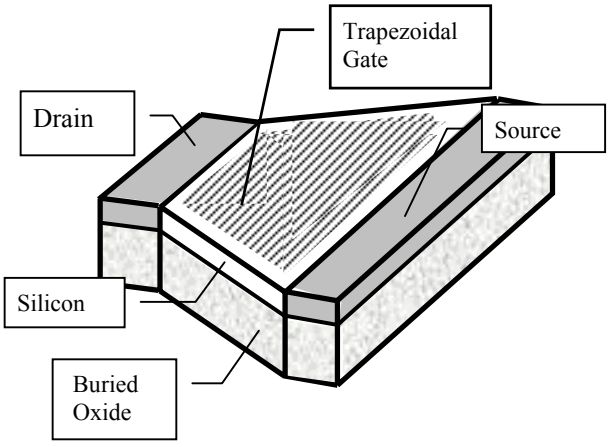

Figure 1 – A schematic view of the ATG SOI NMOSFET.

2. TREE-DIMENTIONAL SIMULATION

The accuracy of the model has been verified based on three-dimensional numeric simulation (TMA DaVinci). In order to facilitate model understanding, some simulation results are showed next. The ATG SOI NMOSFET simulated has a channel length of 1μm, gate oxide thickness t_{oxf} = 15 nm, buried oxide thickness t_{oxb} = 400 nm, silicon film thickness t_{Si} = 80 nm, and a silicon doping concentration Na = 1.0 x 10^{17} cm^{-3}. For the simulations, front and back oxide charge densities of 1.0 x 10^{10} cm^{-2} were used and the interface trap densities were assumed negligible.

The device can be dissected by a vertical longitudinal plane from source to drain, without affecting it's behavior, because no current flows from one half to the other (due

to symmetry). As a consequence, the device drain current is halved. All simulations considered a halved transistor in order to save computational resources. Figure 2 shows equipotential lines in the interface between silicon and gate oxide, when device is in triode region, with 2V applied between gate and source and 1V between drain

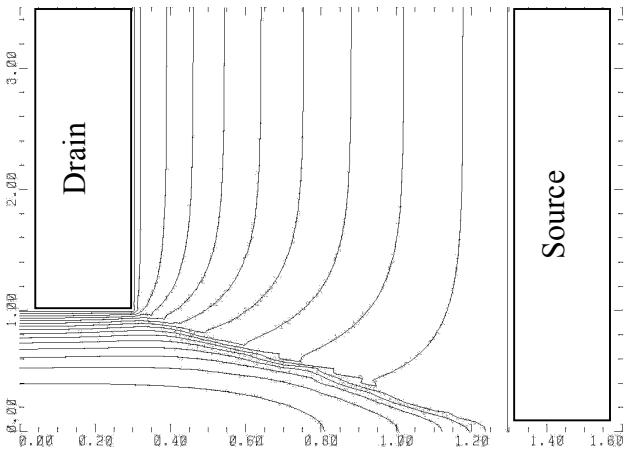

Figure 2 – Equipotential lines in silicon-oxide interface plane (distances in μm)

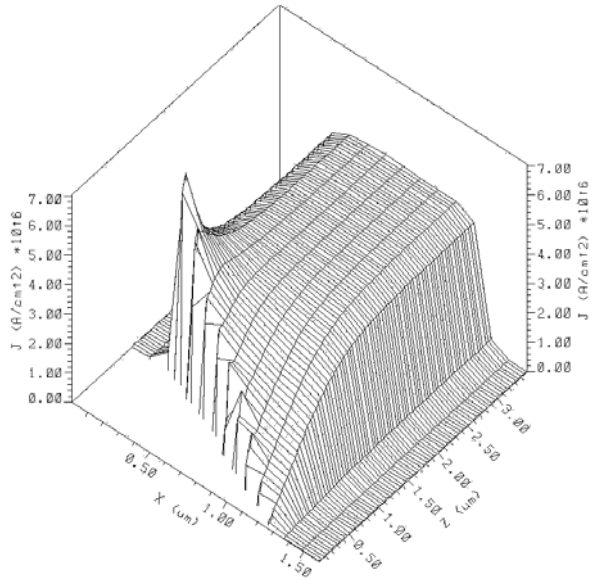

Figure 3 – Current density in silicon-oxide interface plane

and source. Note that all lines are perpendicular to dissection plane and that they are quite straight near the

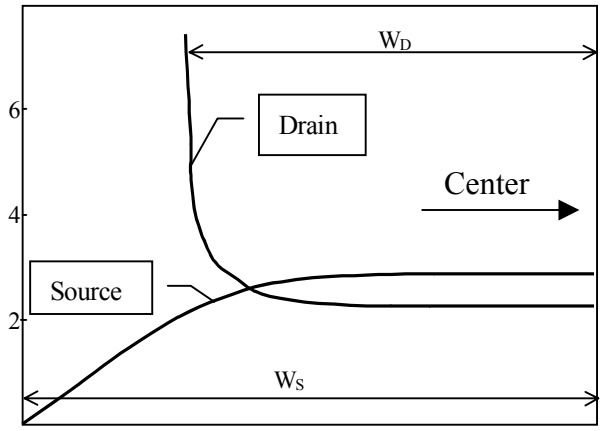

Figure 4 – Current intensity in silicon-oxide interface plane along drain and source interfaces($10^6 A/cm^2$)

center, as if the border effect did not interfere in the center of device. Figure 3 shows a surface plot which represents how drain to source current is distributed in the plane defined by gate-oxide and silicon interface. The peak current occurs at the outer side of drain interface. Figure 4 shows more clearly current density along drain-channel interface and source-channel interface.

3. TRIODE REGION MODEL

Figure 5 shows an elemental section of the highly inverted channel. This section is limited by the lateral edges of channel region and equipotential curves. The 3-D effect will be accounted approximately by using a variable gate width, which depends on elemental-section position:

$$W(y) = 2 \cdot (W_D + \theta \cdot y) \quad (1)$$

where W_D is the drain-side width of the channel and θ is trapezium angle.

Using Ohm's law in an elemental-section:

$$I_D = -2.(W_D + \theta.y)\mu_n.C_{ox1}.Q_{inv}(y)\frac{d\Phi_{S1}(y)}{dy} \quad (2)$$

where μ_n is the mobility of the electrons in the inversion layer, C_{ox1} is the front gate oxide capacitance, Q_{inv} is the front inversion charge, and Φ_{S1} is the potential at the front silicon/oxide interface.

Integrating expression (2) from drain (y=0) to source (y=L), assuming the device is fully depleted, and that the thickness of inversion layer is negligible, leads to the following expression:

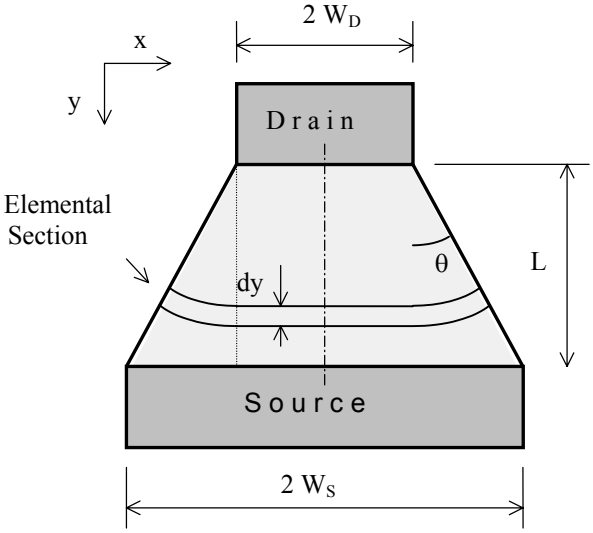

Figure 5 – The elemental section of inverted channel

$$I_D = \frac{2\theta}{\ln\left(\frac{W_D + \theta.L}{W_D}\right)} \mu_n.C_{ox1}. \cdot \left((V_{G1} - V_{th1}).V_{DS} - (1+\alpha)\frac{V_{DS}^{\ 2}}{2} \right) \qquad (3)$$

where α is defined as the ratio between series association of silicon capacitance (C_{SI}) and buried oxide capacitance (C_{ox2}), and gate oxide capacitance (C_{ox1}) in fully depleted devices [3]:

$$\alpha = \frac{C_{SI}.C_{ox2}}{C_{ox1}.(C_{SI} + C_{ox2})} \qquad (4)$$

4. SATURATION

Let's consider initially a rectangular device. In saturation region, the device can be divided in two parts, as can be seen in Figure 6a: a source region, which behaves as the device were in triode operation, and a drain region, where the GCA is not valid. The boundary of the two regions can be determined from an electric field criterion: a line defined by the points in oxide-silicon interface where the horizontal electric field is some previously established fraction of the vertical electric field. The increase in drain current after the transistor enters saturation can be related to the ratio of the length of the device to the length of the source region:

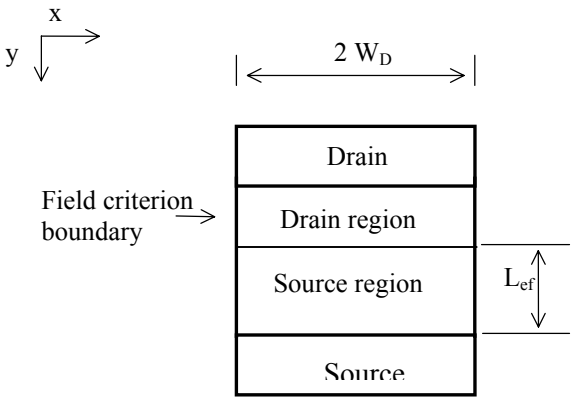

Figure 6a – Drain and source regions in a rectangular device

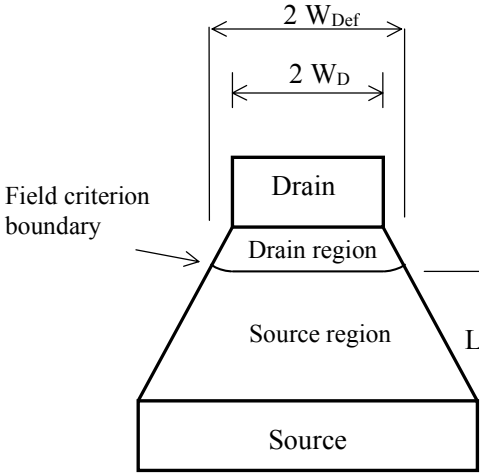

Figure 6b – Drain and source regions in a trapezoidal device

$$I_D = I_{DT}.\frac{L}{L - \Delta L} \qquad (5)$$

where I_{DT} is the maximum triode drain current and ΔL is the drain region length.

Figure 6b shows a saturated trapezoidal device. As can be observed, saturation reshapes the inverted region in a way that W_D/L ratio is effectively increased. Fortunately, increasing this ratio decreases the model's error, as simulation results will show.

Using the conventional approach and defining W_{Def} and L_{ef}, as effective geometric parameters, drain current in saturation region is given by:

$$I_D = \frac{\theta}{\ln\left(\frac{W_{Def} + \theta.L_{ef}}{W_{Def}}\right)} \mu_n C_{ox1}.\frac{(V_{G1} - V_{th1})^2}{(1+\alpha)} \qquad (6)$$

5. SIMULATION RESULTS

Table I shows some values of the shape current gain K_W, defined as the ratio between the trapezoidal-gate device current and a rectangular-gate device with the same drain width (W_D). Observing the table, one can compare the values given by proposed model and the outputs from 3D-simulation for some devices with different geometrical characteristics. The error between these two values (ΔK_W) is also presented in Table 1 and plotted, as a function of θ in Figure 7. The error ΔK_W increases if θ increases and if W_D decreases, due to the border effect. In all range studied, the error is lower than 6.5%. Figure 8 shows a plot of K_W as a function of drain voltage for a device with W_D = 1.5μm, L = 1μm, and θ=45°, and for front gate voltages of 1, 2 and 3V. The shape current gain is not affected significantly by saturation.

Table I: Simulated and modeled K_W.

W_D (μm)	θ (degrees)	K_W		ΔK_W (%)
		3D Simul	Model	
1.5	15	1.07	1.08	0.9
3.5	15	1.03	1.04	1.0
1.5	45	1.19	1.24	4.2
3.5	45	1.08	1.11	2.8
1.5	60	1.23	1.31	6.5
3.5	60	1.10	1.14	3.6

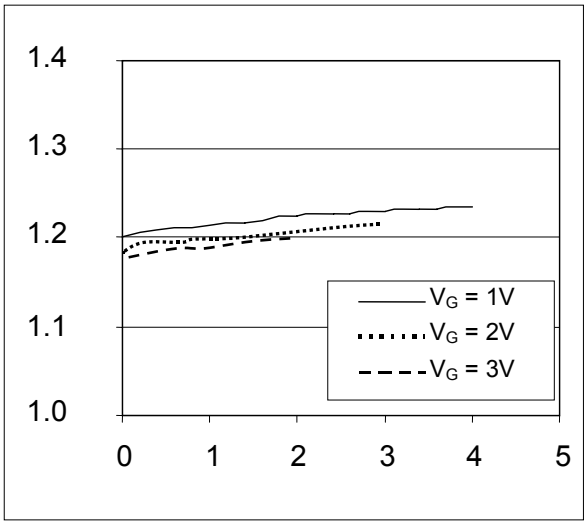

Figure 8 - K_W as a function of drain voltage and front gate voltage (V_G).

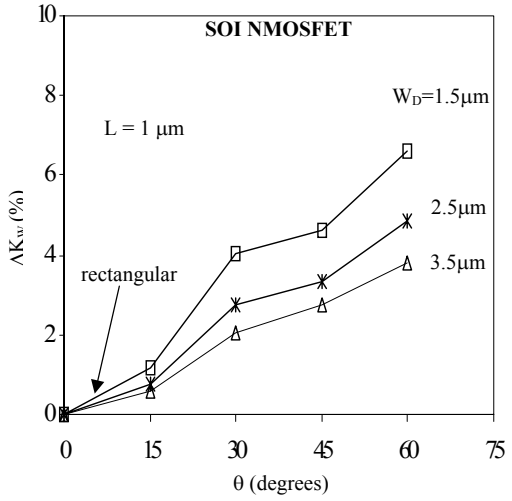

Figure 7 - K_W as a function of θ and W_D.

6. CONCLUSIONS

There is good agreement between the model and the results from 3D simulation for all devices. The proposed model is extremely simple and intuitive, what makes it useful for preliminary projects and for circuit simulation. An immediate application of this proposed simple model is to analyze the current characteristics of edgeless SOI devices, which may be considered as a composition of four ATG transistors with θ = 45°.

7. REFERENCES

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