An Embedded Gate Oxide Short Model for Efficient Electrical Simulation

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ABSTRACT

In this paper a new electrical transistor compact model including a Gate Oxide Short defects is proposed based on a charge sheet model approach. Because this model include Gate Oxide Short defect, it allows to fast simulate realistic digital circuits without any change in the electrical simulation netlist. The basic equations and the topology of the model are presented in details using a charge sheet approach. It is demonstrated that the electrical behavior of the proposed model matches in a satisfactory way the defective transistor behavior.

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Abstract

In this paper a new electrical transistor compact model including a Gate Oxide Short defects is proposed based on a charge sheet model approach. Because this model include Gate Oxide Short defect, it allows to fast simulate realistic digital circuits without any change in the electrical simulation netlist. The basic equations and the topology of the model are presented in details using a charge sheet approach. It is demonstrated that the electrical behavior of the proposed model matches in a satisfactory way the defective transistor behavior.

1. Introduction

The development of CMOS technologies gives the possibility of manufacturing high performance integrated circuits. High accuracy, increased operation speed and reduced power consumption are common device features that can be met using advanced design techniques. However, one ever more difficult demand to guarantee is reliability. Indeed, the probability of a manufacturing defect increases as the circuit density increases and the technology scales down. The testing task typically addresses such an issue.

Test generation for any type of defect is obviously not feasible due to the huge amount of CPU time and memory size required. Instead, test generation relies on fault models that are supposed to both represent the defect behavior and allow easy generation of test vectors. For many years, classical fault models such as stuck-at, stuck-open and stuck-on fault models have been efficiently used. These fault models cover only partially the spectrum of real failures that occur during the manufacturing process of a device. With the increasing demand low ppm defect rates in today's integrated circuits, more accurate fault models are required. In particular, defects that are not correctly represented by classical fault models should be taken into account. It is the case of Gate Oxide Short (GOS) defects that exhibit complex behavior by changing some of the electrical features of the transistor. Moreover, these defects become prevalent defects in today technologies in which devices are scaled down and oxide thickness reduced. The expectation of higher reliability can only be met through the derivation of adequate fault models for this kind of failures. A number of research works have addressed this issue within the ten past years, dealing either with the electrical characterization [1-10] or the modeling [11-18] of gate-oxide shorts.

Both for the characterization and modeling process, one should distinguish between two different types of gate oxide short, i.e. GOS connecting directly the gate to the drain or source or GOS connecting the gate to the channel. For the first type of defect, a realistic model based on the addition of a short resistance between the gate the drain (or source) has been proposed in [12]. For the second type of defect, several models have been proposed based on the split of the faulty device in several smaller devices [11-14]. Although these models perfectly match the electrical characteristics of the defect behavior, they suffer from a strong limitation: they cannot be used to study GOS defects in realistic digital CMOS circuits. Indeed, these models requires to modify the simulation netlist in substituting the original transistor affected by a GOS failure by a lumped element. Moreover these models are unable to deal with minimal length transistor [18]. It is therefore the objective of this paper to present a new model permitting to simulate transistors affected by gate-to-channel shorts without any change in the netlist and able to handle minimal transistor length.

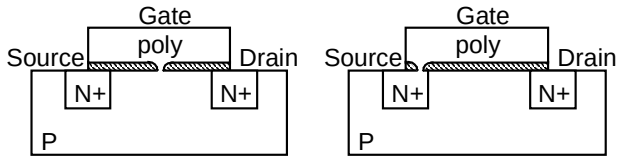
The paper is organized as follows. GOS failures and their associated behavior are described in section 2. Previous defect modeling is addressed in section 3 and sets as reference in order to validate the new compact model. In section 4, we introduce the new compact model approach including the description of the GOS defect. Finally, concluding remarks are given in section 5.

2. Description of the GOS failure

2.1. Defect description

A GOS is a transistor defect that cause a relatively low impedance path between the CMOS gate and the

underlying silicon. Depending on the defect location, the GOS can be seen as a short circuit between the gate and transistor channel or as a short circuit between the gate and drain or source diffusion zones. Figure 1 illustrates these two types of defect. For both types, an undesired path of current through the oxide of the gate appears thus creating a violation of the gate isolation principle. It is generally admitted that GOS may have different origins such as lithographic defect on mask, field failure due to EOS, ESD…



(a) gate-to-channel (b) gate-to-source (drain)

Fig.1: Pinhole in a MOS gate

2.2. Defect behavior

One of the main specificity of a GOS defect is that the pinhole that shorts the gate to one point of the underlying silicon creates a new device in which an important gate current can flow. It is therefore possible to study the IG vs VG characteristics of a defective transistor. As commented by the authors of many previous papers [1-3], two distinct electrical behaviors are observed depending on the defect type. The first type of defects connecting the gate to drain or source diffusion zone is referred as an ohmic defect and exhibits a linear behavior in the IG vs VGS characteristics. In contrast, the second type of defects connecting the gate to transistor channel exhibits a non-linear behavior in the IG vs VGS characteristics. This paper concentrates on this non-linear case. Figure 2 shows typical IG vs VGS characteristics for the non-ohmic types of defects.

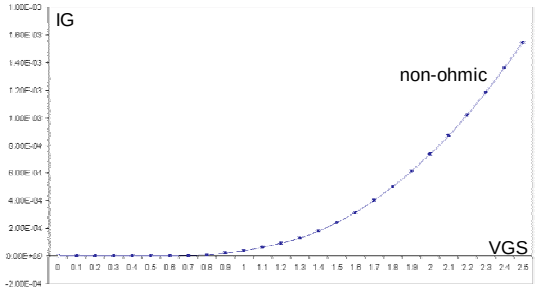
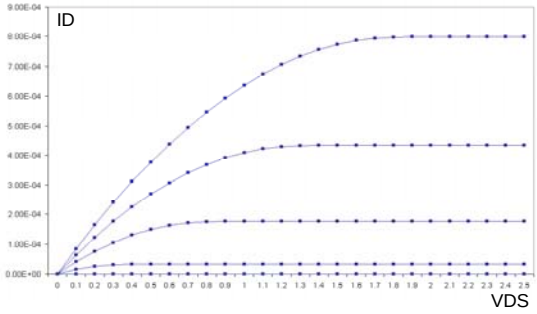


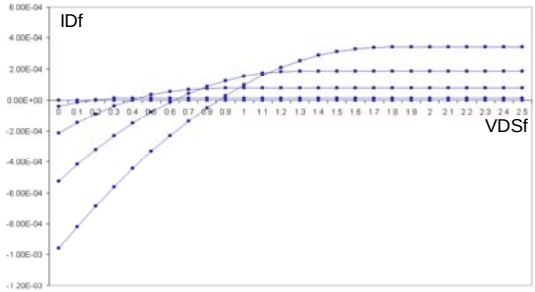
Fig.2: IG vs VGS characteristics of a MOS with a GOS

Regarding the ID vs VDS characteristics, all experiments have demonstrated that the drain current of a defective transistor only slightly resemble the typical MOS transistor drain current. Figure 3.a and 3.b show the typical ID vs VDS characteristics of non-defective and defective transistors. Basically, the defect manifests itself through two main phenomena:

- reduction of the maximum drain current at high VDS,
- appearance of a negative drain current when VDS is small in comparison with VGS.



(a) non-defective NMOS



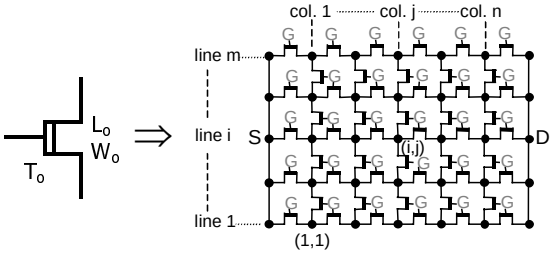
(b) NMOS with a gate-to-channel GOS

Fig.3: ID vs VDS characteristics

3. Electrical Non-Linear Split MOS Model

3.1. Model description

In order to study GOS defects connecting the gate to the channel, an electrical model of the fault-free transistor based on a lumped-element model has been proposed in [11]. In this model represented in figure 4, the non-defective channel is split and become a two-dimensional array of MOS transistors.



(a) original MOS (b) 5x5 split model

Fig.4: Split model of a non-defective NMOS

As an example, we consider an original transistor T_o with L_o=2.1 µm and W_o=3.5 µm in a 0.25µm technological process. This transistor can be split in a 5x5 network of elementary NMOS transistors designed at length L_i=0.37µm and W_i=0.4µm. As illustrated in figure

5, a good agreement is observed between the simulated IDS vs VDS characteristics of the 5x5 network and the original transistor.

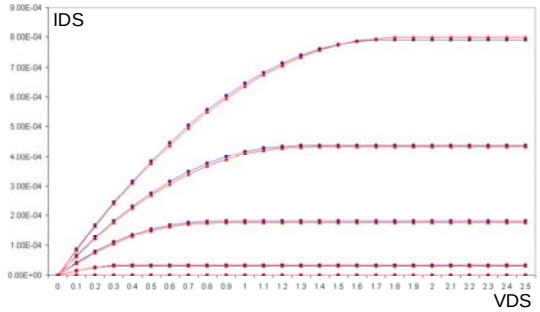


Fig.5: Comparison of the IDS vs VDS characteristics of the original transistor and the split MOS model

Based on this lumped-element model, a GOS defect can be introduced in the transistor by connecting a short resistance R_{GOS} between the common gate G and one of the internal nodes of the network, denoted (i_f,j_f). Figure 6 gives an example of a central defect introduced in the transistor. The defect resistance and location can then be varied through the value of R_{GOS} and position (i_f,j_f) in the network.

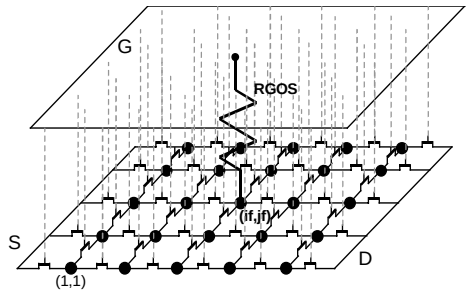
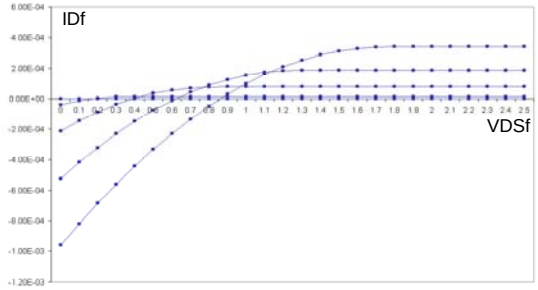
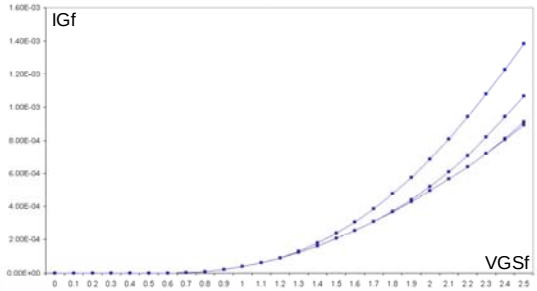


Fig.6: Split model of a NMOS with a GOS

This model has been demonstrated to describe in a satisfactory way the electrical behavior of gate-to-channel shorts [8-9]. For illustration, figure 7.a shows the simulated ID vs VDS characteristics of a defective transistor with a 1Ω central defect. This model also permits to simulate the IG vs VGS characteristics, as depicted in figure 7.b. Note that these characteristics are in agreement with the experimental behavior observed for gate-to-channel shorts (see figure 2).



(a) ID vs VDS characteristics



(b) IG vs VGS characteristics

Fig.7: Simulated I-V charateristics of a defective NMOS using the split model

3.2. Model limitations

As described in the previous section, the split MOS model for GOS describes describe in a satisfactory way the behavior of gate-to-channel defects and for this reason has been widely studied by different authors [8-14]. However this model suffers from severe limitations as discussed below.

As everybody knows, SPICE like simulations are performed using card models describing the transistor parameters in the targeted technological process. Using these card models, transistors of any length can be simulated as far as they are larger than the minimum (L_{min}) allowed by the technological process. Any attempt to simulate transistors smaller than the minimum would make the simulation results (if any) unreliable. Consequently, when using the split MOS model for simulating GOS defects, the elementary MOS transistor obtained after the splitting of the original transistor cannot have a length smaller than L_{min}. This obviously implies that the original transistor cannot be at minimum length. Even the smallest network composed of two transistors in series as suggested in [13-14] corresponds to an original transistor with length equal or higher that $2L_{min}$. It is therefore impossible to study minimum transistors affected by GOS failures using a split MOS model. This is the first extremely strong limitation taking into account that in a classical digital cell library, all transistors are designed at minimum length. In this context, although the split MOS transistor permits to accurately model the defect behavior, it clearly appears inadequate to simulate GOS defects in realistic digital circuits. According to the previous remarks, an electrical model of GOS transistor has been proposed in [18].

Moreover, when simulating a transistor affected by a GOS defect, the netlist has to be modified in order to substitute the original transistor with a lumped element. This change has for consequence a significant overhead in simulation time which may represent a real problem when dealing with fault injection in large digital circuits.

4. Compact MOS Model including GOS

4.1. Classical Model Formulation

This section summarizes the fundamentals of the charge sheet approximation used to develop classical MOS model. The main advantage of this approach is to be able to describe the device characteristics in all the operating regimes without introducing discontinuities in the drain current and its derivatives with respect to bias voltages [19]. In this approach, the charge neutrality is applied to determine the surface potential from which all of the main model electrical variables can be calculated. The calculation of the surface density of charge Qsc in the semiconductor is performed from the Poisson equation and the Gauss theorem. This calculation leads to the following analytical expression of Qsc:

$$Qsc=-\gamma\cdot Cox'\cdot\sqrt{\psi s-Vth\cdot\left[\exp\left(\frac{\psi s-2\cdot\psi b-Vy}{Vth}\right)-1\right]} \quad (1)$$

where γ, Cox', Vth, Ψs, Ψb, Vy are respectively the substrate effect coefficient, the gate oxide capacitance per unit area, the thermodynamic potential, the surface potential, the bulk Fermi level and the potential along the channel.

The charge density in the substrate Qb has also to be taken into account with the assumption that the doping is uniform with an abrupt profile. The expression of Qb is given bellow:

$$Qb=-\gamma\cdot Cox'\cdot\sqrt{\psi s-Vth} \quad (2)$$

The expression of the density of charge in the channel Qn is derived from the expression of the density of charge in the semiconductor Qsc and in the substrate Qb.

$$Qn=Qsc-Qb \quad (3)$$

Finally, the charge density on the gate Qg is given as follow, where vfb is the flat band potential:

$$Qg=Cox'\cdot(Vg-vfb-\psi s) \quad (4)$$

Using the relationship (charge conservation) between Qsc and Qg, the surface potential Ψs, can be obtain implicitly with the following equation:

$$G(\psi s)=Qsc(\psi s)+Qg(\psi s)=0 \quad (5)$$

The surface potential near the drain Ψsd and the source Ψss are obtained in using the above equation (Equ.5) in which Vy is replaced by VD and VS respectively. Knowing the surface potential, the current equation Id that takes into account the drift and diffusion components is given bellow:

$$Id=\mu\cdot Cox'\cdot\frac{W}{L}\cdot[F(\psi sd)-F(\psi ss)] \quad (6)$$

with

$$F(\psi s)=(Vg-vfb+Vth)\psi s-\frac{\psi s^2}{2}-\frac{2}{3}\cdot\gamma\cdot\sqrt{\psi s-Vth}\cdot\left(\psi s-\frac{5}{2}\cdot Vth\right) \quad (7)$$

where μ, W, L are respectively the effective carrier mobility, the width of the transistor and L the length.

Concerning the dynamic behavior of the intrinsic model, the non quasi-static approximation is used. This approach is based on the charge neutrality in the structure [20].

4.2. Modified Model Formulation - GOSMOS

In order to take into account the GOS defect behavior in the MOS compact model description, some modifications have to be introduced in the model formulation.

The first modification is directly linked to the introduction of the GOS defect in the MOS structure. Knowing that a pinhole in the oxide is a completely random defect in terms of resistance value, localization and size, our model must be able to describe all this parameters. To do so, four new parameters are included in the model cart as follow:

- *dw* is the percentage of the transistors width affected by the defect,
- *dl* is the percentage of the transistors length affected by the defect,
- *lp* is the position of the center of the defect with the source as reference,
- *ro* is the resistivity of the pinhole.

With this new parameters, the resistance of the defect is calculated with the equation given bellow, where tox is the oxide thickness:

$$Rgos=\frac{ro\cdot tox}{(W\cdot dw)\cdot(L\cdot dl)} \quad (8)$$

When studying GOS defect, it clearly appears that the impact of the defect is bi-dimensional, i.e. on the width as well as on the length of the transistor. The classical equations are build only in considering the charges and the surface potential along the length of the transistor. Consequently and in order to take into the dependences on the width dimension, three currents I1, I2 and I3 are defined in the structure, as follow:

- I1 is the current in the defect free part of the channel,
- I2 is the current between the drain and the defect,
- I3 is the current between the defect and the source.

The last modification concerns the variation of the surface potential along the channel in the perimeter of the defect. So in order, to take into account this variation, the

calculation of the surface potential is not only performed near the drain (Ψsd) or the source (Ψss), but also near the defect center. This surface potential is named Ψsc and is obtained in using the equation (5) in which Vy is replaced by VC, with VC the potential between the node represented by the defect localization on the channel and the bulk.

Considering all these modifications, the new currents equations are given as follow:

$$I1=\mu 1\cdot Cox'\cdot\frac{W\cdot(1-dw)}{L}\cdot[F(\psi sd)-F(\psi ss)] \quad (9)$$

$$I2=\mu 2\cdot Cox'\cdot\frac{W\cdot dw}{\left[L-lp-\frac{L\cdot dl}{2}\right]}[F(\psi sd)-F(\psi sc)] \quad (10)$$

$$I3=\mu 3\cdot Cox'\cdot\frac{W\cdot dw}{\left[lp-\frac{L\cdot dl}{2}\right]}[F(\psi sc)-F(\psi ss)] \quad (11)$$

The mobility μ1, μ2, μ3 are calculated separately in order to take into account the different length and surface potential for each current.

The last current expression in our model, is the one of the current Igos between the gate and the channel, which is defined below:

$$Igos=\frac{VG-VC}{Rgos} \quad (12)$$

The potential VC is calculated numerically in solving the implicit equation given bellow:

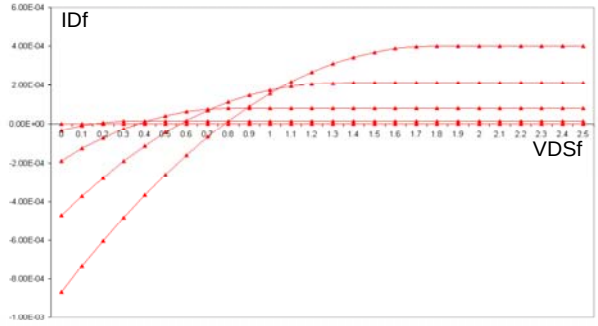
$$Igos+I2-I3=0 \quad (13)$$

This equation (Equ.13) is obtained by applying the node law at the defect center in the channel.

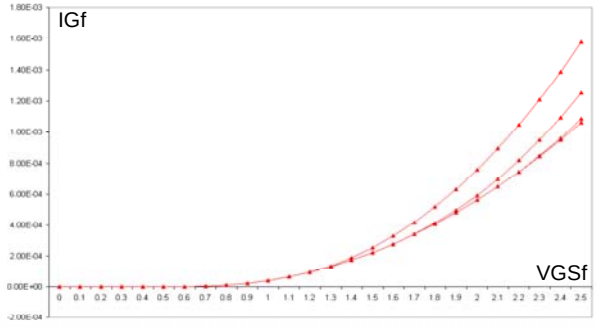
Finally, the dynamic behavior is based on the non quasi-static approximation. But in our modified description, the charge are calculated in three part using the surface potential near the defect.

4.3. GOSMOS Simulation results

Our new compact MOS model called *GOSMOS* has been implemented for the electrical simulator ELDO using the HDLA language.



(a) ID vs VDS characteristics



(b) IG vs VGS characteristics

Fig.8: Simulated I-V charateristics of a defective NMOS using the GOSMOSmodel

Using the *GOSMOS* model, simulation of ID vs VDS and IG vs VGS are performed for a L=2.1 μm and W=3.5 μm transistor in a 0.25μm technological process. The figure 8.a shows the simulated ID vs VDS characteristics of a defective transistor with a 1Ω defect. The figure 8.b illustrates the characteristics of IG vs VGS in the same condition. These characteristics are in a good agreement with the experimental behavior observed for gate-to-channel shorts (see figure 2) and with the ones obtained with the split model (see figure 7).

Moreover, when simulating I-V characteristics of a transistor affected by a GOS defect, the simulation performed with a 5×5 split model is 50 time slower than the one performed with our *GOSMOS* model.

In term of netlist change, the original transistor model has to be replaced by the *GOSMOS* one and the parameters of the defect have to be set, like in the example given bellow:

Transistor call: m1 d g s b MOS W=Wo L=Lo
Modified call: m1 d g s b GOSMOS W=Wo L=Lo
+ dw=DWo dl=DLo lp=LPo ro=Roo

Consequently, this model allows to perform fast generation and simulation of GOS defect in large digital circuit. Both properties are extremely important when dealing with fault injection. Moreover, the complete tuning of the resistance value, of the size and location of the defect allows to precisely study the impact of a large set of GOS defect for a given transistor.

5. Conclusions

In this paper, we proposed a new compact MOS model for gate-to-channel GOS defects. The fundamental idea is to obtain a complete compact model that enable to fast simulate a large set of GOS defects in realistic digital circuits without any netlist change. Based on a classical

charge sheet approximation, we developed a complete compact model that include a GOS defect in its formulation. The model is constructed as follow:

- Introduction of the new cart-model parameters to define the geometry of the defect,
- Calculation of different current to take into account the bi-dimensionality of the defect.
- Calculation of the surface potential at the defect location
- Calculation of the current Igos through the defect.

It has been shown that the behavior of the proposed model matches in a satisfactory way the behavior of a defective transistor model. The main advantage of the *GOSMOS* model is to be build with a surface potential approach and so to ensure the continuity of the device characteristic in all regime of operation. Moreover, it allows fast simulation time compared to previous approach and a complete tuning of the defect characteristics.

Finally, future work will concentrate on the study of the defect model parameters to reproduce GOS defects of various resistance, location and size and to examine their impact on the static as well as dynamic behavior of the transistor.

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