FAULT DETECTION IN ALGORITHMIC ADC MONITORING DYNAMIC CURRENT IN SI CONVERTERS AND CHARGE IN SC CONVERTERS

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ABSTRACT

Fault detection in analog to digital converters is a difficult task that can been enhanced with the application of Built-in Sensors. The special capability of dynamic current sensors, that include the capability to process the highest frequency components in the dynamic power supply current, to detect fault in SI algorithmic analog to digital converter, with a relative reduce area increments in the design of the ADC, is compared with sensors of charge in switched capacitor circuits establishing a correlation between the type of signal mainly used in the converters and the parameter measured to detection of faults.

A relative comparison between the efficiency and area used by the sensors in the two types of fault detection method is presented in this paper. The processing of the sensor captured signals to determine the go /no go post fabrication test are also considered in the paper in both type of algorithmic analog to digital converters.

The different topologies of algorithmic switched current cyclic or redundant signed-digit cyclic(RSD) ADCs, goes from those architectures based on SI and S^2I memory cells, to fully differential ones for this type of ADC circuits. All of this architectures for cyclic algorithmic ADC are developed to achieve a higher level of analog performance and reduction of influence of the most common error in the circuits.

An algorithmic redundant cyclic (RSD) switched capacitor ADCs fully differential has been designed as well, as a SC benchmark circuit to compare the test results with the switched current ones.

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A comparison between the efficiency and area used by the sensors in the two types of fault detection method is presented in this paper. The processing of the sensor captured signals to determine the go /no go post fabrication test are also considered in the paper in both type of algorithmic analog to digital converters.

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1. INTRODUCTION

In this paper we will study switched current and switched capacitors cyclic or RSD algorithmic A/D Converters. In the first case the implementations based on SI topologies support the idea that the current mode approach yields small area, low power but, however, accurate (12 – 14 bits) A/D Converters. In the second case an standard SC fully differential implementation has been used in many application during the last years.

In spite of the visible benefits in the SI case of low cost (use of standard digital CMOS processes to implement the analog part of the converter), high speed (inherent low impedance) and low supply voltage (does not limit the signal range) obtained with these circuits in the implementation of A/D Data Converters; there are some limitations of precision, linearity and noise in these kind of discrete circuits which are the reason why switched current technique has not become yet an industrial standard.

Nevertheless, in the evolution of switched-current circuits the design of the memory cells has been improved, reducing the working errors due to the non-ideal characteristics of their components. In this way the S^2I cells achieve better error corrections than those obtained with the introduction of feedback techniques with operational amplifiers in the basic SI cells, since the resultant circuit is simpler. Nevertheless, it is possible to further reduce the errors produced in the operation of the S^2I cells by incorporating cascode designs or introducing feedback amplifiers giving rise to S^3I cells, which although increasing the complexity reduce some of the error sources by various magnitude orders.

Furthermore, fully differential and balanced structures have been developed to improve the performances of SI circuits [11]. These architectures are frequently employed to achieve the highest level of analog performance in both switched-capacitor and continuous-time circuits. These topologies reduce distortion by cancelling even-order harmonics and reduce also cross-talk from neighbouring digital circuits through common-mode and power supply rejection of the amplifiers. However, the accuracy and linearity are still inferior to what can be reached by switched-capacitor technique, mainly due to the nonlinearity error caused by the charge feedthrough effect. Moreover, the designs are rather simple since they have either no common-mode feedback or a common-mode feedback circuitry that will

introduce some differential-mode error due to the element mismatch.

Nevertheless as the industrial position of the SC designs is stronger than the SI designs, the possibility to implements an algorithmic analog to digital converters is now open to SI or SC design styles

Due to all these reasons and the strong industrial position of the SC designs, we have compared the inclusion of built-in sensors and the test results in both design styles.

The high cost associated with production and the field test of complex mixed signal VLSI circuits make attractive the alternative to simplify the test equipment moving some or all the tester functions onto the chip. This highlights the advantages of the fault detection method based on built-in current or charge sensors.

As the power supply current Idd can be defined by its two elements, Iddq-quiescent current and Iddt-transient or dynamic current, many published papers in the last years have dealt with the design of sensors specialised in both types of current detection. Nevertheless, there are hard-to-detect faults in continuous time circuits and also in switched analogue circuits that need an improvement in the detection methods to enhance their fault coverage.

In the SC circuits we have considered to use a charge sensor relating the parameter to measures to detect the faulty circuits to the main signal activity in the SC circuits as it is the charge transfer within the circuits.

Catastrophic models include short and opens as most of the defects that exist in CMOS IC mixed signals circuits, however, open defect, the open source/drain or the floating gate, can generate complicated fault effects and sometimes are difficult to detect with the direct measurement of the power supply current.

In the paper we use a sensor to det4ct fual in the SI circuits relying on the voltage drop across a resistance, induced by the dynamic power supply current, which has the additional capability of analysing changes in the slope of this current due to some hard-to-detect circuit faults, in order to enhance the fault coverage of the test process.

This last operation of the sensor gives greater specific weight to the higher frequency components of the current. Thus, an inductive rather than a resistive load is used to carry out the conversion of the current sampled in the CUT to a voltage. To design the inductive load a simplified structure of a gyrator and a capacitor is used, made up of four transistors.

In fact, the main idea proposed in this work is based on a sensor capable of detecting faults in the basic SI and S^2I cells, in the fully differential SI cell, and in the specific current copier cells, which develops the dynamic current test on switched current cyclic or RSD algorithmic A/D Converters.

This type of built-in dynamic current sensors applied to SI algorithmic A/D converters allows a low cost post-fabrication test of these circuits, where a high fault coverage is achieved, due to the fact that an important part of the test cost is absorbed by the built-in sensor.

In the SC circuits we have study a charge sensor as the most suitable methos to deted fualts in thes type of circuits. In this case a low cost post-fabrication test of these circuits, where a high fault coverage is achieved, as in the SI circuits.

The paper is organised as follows. Section 2 describes the operation of the SI cyclic algorithmic AD converters based on two current mode architectures: SI and S^2I, fully differential. Section 3 describes the resistive and slope-sensitive dynamic current sensor which emulates the behaviour of series circuit composed of a resistor and an inductance connected to ground, and explains how the BICS is coupled to the benchmark circuits. Section 4 describes the operation of the SC cyclic algorithmic AD converters based on a simplified fully differential architecture. Section 5 describes the charge sensor and explains how the BICS is coupled to the benchmark circuits.

Section 6 describes the fault evaluation process and some simulation results are shown in order to verify the efficiency of the test approach. Finally, some conclusions are presented.

2. SWITCHED-CURRENT CYCLIC ALGORITHMIC A/D CONVERTERS

The first structure analysed is based on an cyclic algorithmic approach [8] which gives attractive properties to the implementation, medium speed, small area and the use of few MOS transistors, although it introduces a complex switching schedule. This algorithm has a maximum resolution of 14 b and presents linearity errors below 1 LSB.

The algorithm follows the formula:

$$D_i = 1, \text{ if } s(t) \geq W_{i-1} + I_{ref}/2^i, \text{ else } 0$$

$$W_i = W_{i-1} + D_i\, I_{ref}/2^i$$

The schematic of the circuit designed for this A/D Converter can be seen in Figure 1.

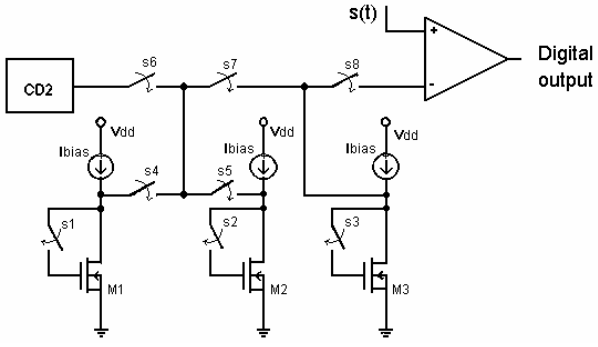

Figure 1. A/D Converter

As it can be seen in figure 1, the sampled analog signal is applied to the comparator during the whole conversion cycle. First, the successive I_{ref} dividing circuit, CD2 loads the value of I_{ref} into the transistor M_3. Then, this current is compared with the sampled signal in such a way that the comparator output is 1 if the sampled input is higher than the reference current or 0 in other case. So we have just obtained the MSB of the digital output D_0. After that, if $D_0 = 1$, the intermediate value W_0, I_{ref} in this first cycle, is stored in M_1 and CD2 loads M_2 with $I_{ref}/2$ and these values are added, stored in M_3 and compared with the sampled input again in order to obtain D_1. If $D_i = 0$, the intermediate value W_i is maintained in its previous value W_{i-1}. This scheme is repeated for the rest of the N-1 bits until the digital word is completed.

The second algorithm structure is based on the redundant signed-digit (RSD) cyclic algorithmic conversion with the division principle developed in [12], which consists on the multiplication by two of the signal to be converted, followed by a comparison of the result with a reference current.

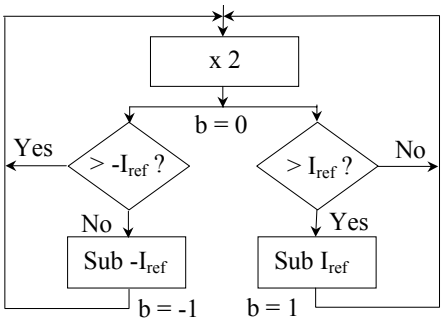

Figure 2. RSD approach

Following figure 2, if the input signal multiplied by two is higher than the reference, the MSB of the digital output is set to 1 and the reference is subtracted from the input; otherwise, the MSB is set to 0 and no arithmetical operation is done. The remaining part of the input signal is called residue current and undergoes the same operation in order to obtain the rest of the bits of the digital output.

Until now we have introduced the principles of two cyclic algorithmic A/D Converters, made of basic switched current cells or current copiers.

Furthermore, it is possible to improve the performance of these SI circuits by applying S^2I and fully differential structures by introducing these kind of enhanced memory cells as storage units or current copiers.

The development of fully-differential storage units has been mainly thought to keep the clock-feedthrough error to a constant and the linearity of the storage unit not affected by this error. In other words, the enhancement of storage units by applying fully differential topologies tries to further alleviate the clock-feedthrough error effects, since the complete elimination of charge injection errors is almost impossible.

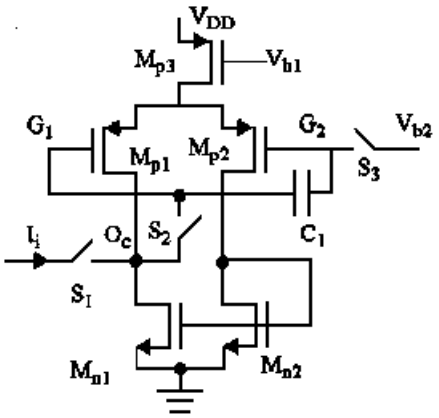

Figure 3. Differential-pair DP

Figure 3 shows the differential-pair storage unit (DP) proposed in [10]. In the sampling state the input current I_i is stored by turning on switches S_1, S_2 and S_3 feeding I_i to M_{p1}, M_{p2} and C_1. The capacitor charges up to whatever gate voltage is needed by M_{p1} and M_{p2} to support a current difference of I_i. This topology produces that the clock-feedthrough of switch S_2 do not contribute to the charge injection because, so as to sample the stored current in the operation state, the switch S_3 is turned off a little bit earlier than S_1 and S_2 so that the capacitor C_1 is floating. In fact, the only contribution to charge injection comes from S_3.

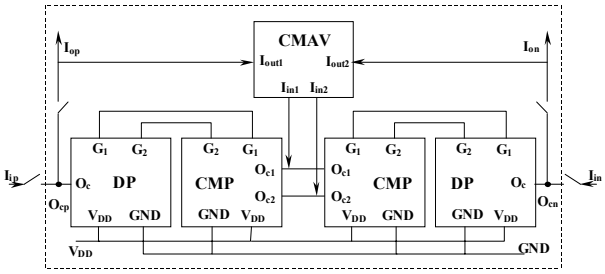

Figure 4. Balanced differential-pair storage unit

Figure 4 shows the scheme of a balanced differential-pair storage unit [10] based on the DP presented. This current cell is comprised of two DPs, each of them with a common-mode feedback differential-pair CMP, to control the common-mode. The common-mode averaging block CMAV contains switches for connecting I_{in1} to Out_1 (or Out_2) and I_{in2} to Out_2 (or Out_1) in a time-multiplex way, and it eliminates the differential-mode error introduced by the difference of the common-mode feedback.

As far as the S^2I cells, used as current copiers, is concerned, in Figure 5 we show a cascode S^2I current memory cell, consisting of two pMOS transistors and another two nMOS transistors, which make up the fine and coarse current

memories respectively. This type of memory cells significantly reduces the most frequent errors in the SI cell [2].

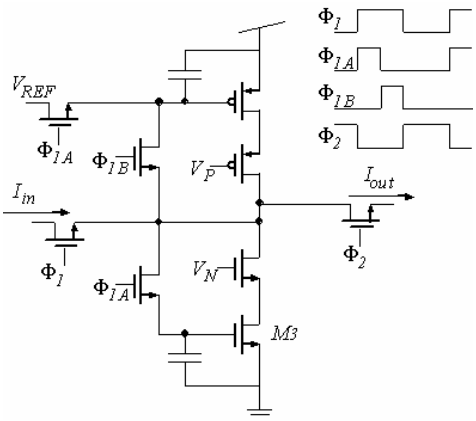

Figure 5. Cascode S^2I cells and clock phases

3. DYNAMIC CURRENT SENSOR

In analogue continuous-time circuits a dynamic supply current coupling method has been proposed based on a current mirror and taking advantage of the parasitic capacitance associated with these structures[1].

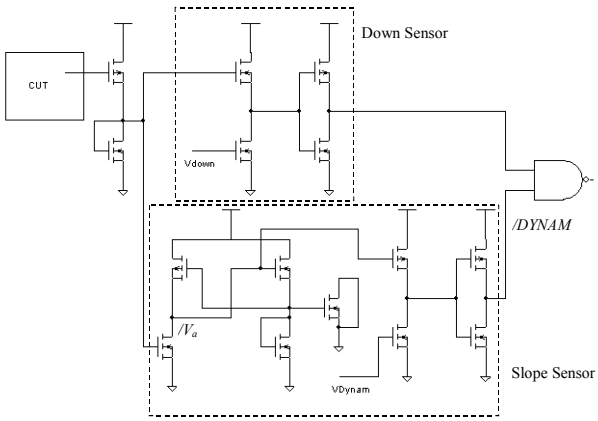

Figure 6. Dynamic sensor

In Figure 6 a resistive/inductive sensor has been implemented. In the upper branch the sensor capture the dynamic current through the analogue circuit, by means of an additional branch of the current mirror placed in parallel to a biasing branch of the CUT. The test circuitry converts this current into a binary voltage.

As the current captured may increase or decrease in the faulty circuits, with reference to the fault-free one, we firstly designed a sensor that detects the current's upper and lower limits. This has been designed, as shown in figure 6, to detect the presence of a fault when there is an increase or a decrease of the current consumption. Nevertheless some faults are not detected, for example, the short drain-source in cascode transistors of a S^2I cell.

It is possible to detect this type of faults if we consider the dynamic current in the coarse memory MOS transistor. In this case the slope of the dynamic current is different in the fault free circuits and in the faulty circuit.

It could be possible to redesign lower branch of the sensor to detect this type of faults if we consider the response of the sensor to dynamic currents.

The enhanced built in current sensor (BICS) proposed for the detection of the hard faults in the CUT is based on the additional analysis of the slope of the dynamic power supply current. Therefore, it is necessary to design a circuit which presents a frequency dependency, in such way that the circuit amplifies the highest frequency components most. This is the behaviour of a series circuit composed of a resistor and an inductance connected to ground[1].

4.-SC FULLY DIFFERENTIAL ALGORITHMIC ADC

The SC algorithmic fully differential RSD analog to digital converters used as a benchmark circuits is presented in the figure7

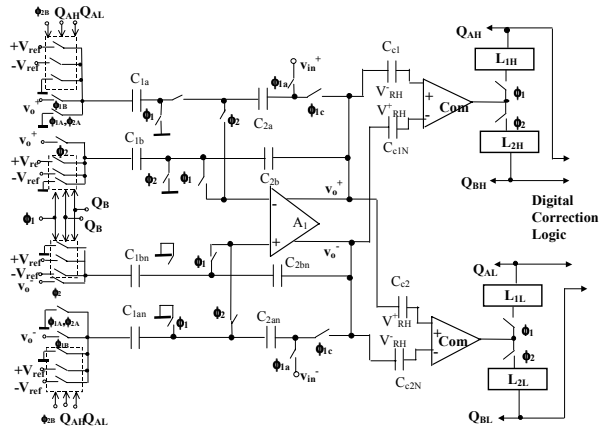

Figure 7: SC Fully differential algorithmic ADC

These circuits include digital techniques to correct finite gain amplifier, offset and the switch feedthroug errors. .Nevertheless one of the most efficient method to correct these errors is to modify the algorithm and to introduce the RSD converter type.

The RSD converter is based on the digital division Sweeny-Robertson-Tocher algorithm, adapted to an A/D converter, including in the cyclic algorithmic comparator two level of de comparison, one positive P and another negative Q, in this way the most commons errors are reduced or compensated. The algorithm operation is represented in figures 8

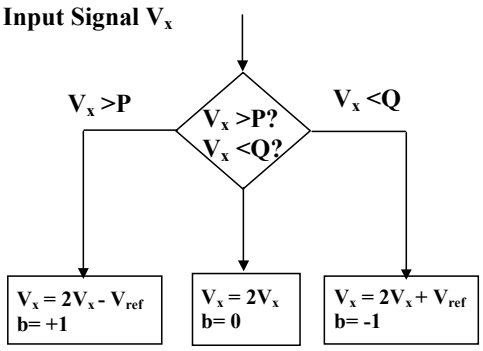

Figure 8 RSD algorithm

5.- CHARGE SENSOR

A charge sensor which have the capability to detect dynamic current changes have been used as a starting point to apply this type of monitoring to SC analog circuits [13] and it is presented in figure 9.

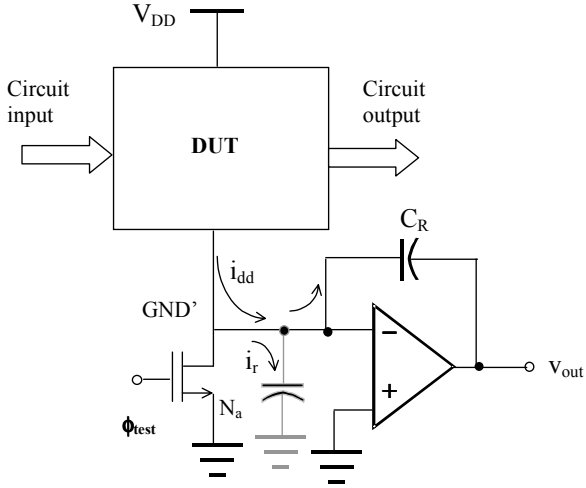

Figure 9: Charge sensor

The operational amplifier used in this sensor is presented at the level of circuits in figure 10.

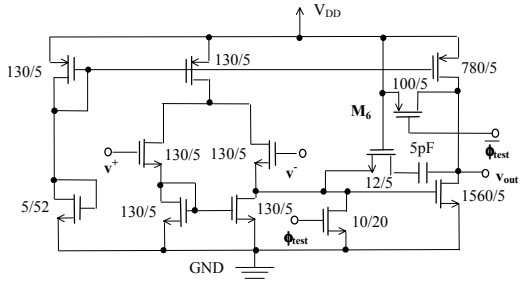

Figure 10 Operational amplifier

It have proved[13] that the voltage of the GND' during a fault free operation of the DUT is

$$V_{GND'} = \frac{1}{(1+A)C_R}\int_{Per} i_{dd}dt = \frac{Q_{no\ def}}{(1+A)C_R}$$

The output voltage of the sensor

$$V_o = V_{dd} - \frac{A}{(1+A)C_R}\int_{Per} i_{dd}dt$$

And in a fault free circuit the sensor output voltage will range between the values

$$V_o = V_{dd} - \frac{Q^{max}_{no\ def}}{C_R} < V_o^{no\ def} < V_{dd} - \frac{Q^{min}_{no\ def}}{C_R}$$

$Q^{max}_{no\ def}$ is the minimum charge driven in a defect free circuit during a transition.

A fault is detected when the sensor output voltage lies out the limits defined.

6. FAULT EVALUATION OF THE TEST APPROACH

The simulations have been carried out, both on the first algorithmic ADC described in section 2, also considering the improved designs including S^2I and fully-differential cells.

The catastrophic fault model considered includes shorts between the gate and the source/drain of the transistors, together with opens in the source/drain contacts[4]. However it has been reported that the floating gates are important faults within transistor opens[5]. In this work it has been considered that all the faults have the same probability of occurrence. The catastrophic transistor level fault model has been used for the fault simulation. The shorts are modelled by a 100Ω resistor.

The open faults are modelled by a 10MΩ resistor in parallel with a 1fentoFarad capacitor. Although in [6] it has been demonstrated that the open gate defect strongly depends on the technology and physical topology of the circuit, this widely-used model helps the convergence of the electrical simulator and the repetitive results obtained can be used to evaluate the efficiency of the proposed test methodology.

Nine different faults of gate oxide short (GOS) between gate and bulk for each nMOS transistor, and three GOS faults for each pMOS transistor have been considered [7], which cover the range from the hardest to the softest situation of GOS, corresponding to three values of R_s (1Ω, 1KΩ, 1MΩ) and K (0.1, 0.5, 0.9).

As far as the test stimuli is concerned, in the case of continuous circuits, it is necessary to apply a pulse at the input to provoke a transient at the output. However, in this type of discrete circuits, the changes in clock phase are taken advantage of, and so, it is sufficient to apply a constant signal at the input to be able to detect the presence of a fault.

The parameters measured were: the voltage /V_a, obtained from the conversion of the supply current with an inductive load, and the voltage obtained from the conversion of this current with a resistive load.

In this way, the value of the two parameters will determine the presence of a fault in the dynamic stage and/or in the static stage of our sensor, respectively.

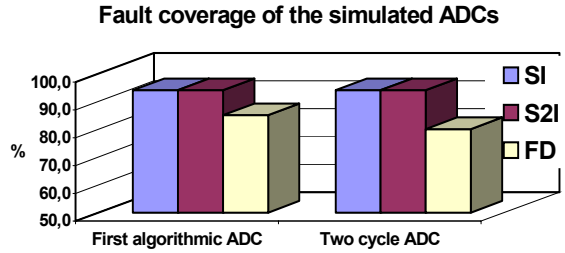

Figure 11. Fault coverage of the ADCs

Figure 11 shows the fault coverage obtained with our test approach in the faulty cases simulated for the two different cyclic algorithmic AD Converters studied, and the three possible topologies for each one: SI, S^2I and fully-differential storage units.

The sensor detects more than 80% of the simulated faults in all the designs studied. However, the fully-differential structures, due to the increased complexity of the circuits and some problems of fault reflection from one cell to the next, have a fault coverage almost 10% lower than the SI structures.

It is important to point out that there are some faults in any of the current cell topologies that are not reflected in the behaviour of the rest of current copiers of the A/D Converters. That is the case of those faults that do not produce any increase or decrease in the supply current, but a change in the slope of this current.

For that reason, if we are monitoring the supply current in the last current copier, we will be able to detect only those faults that produce an increase or decrease in the supply current of the previous cells; owing to the fact that they modify the output current of those cells. However, those faults in the last current copier that produce a change in the slope of the supply current could be detected.

For example, for the S^2I topologies, the fault coverage obtained is near 94% for that reason. Nevertheless, if we modify the connections of the dynamic current sensor in such a way that, by the use of switches, and during different clock phases, we measure the supply current in all the current cells, we will be able to detect 100% of the shorts and open faults that could appear in any of the current copiers.

As far as the algorithmic design is concerned, the best results have been obtained for the first algorithmic approach, with an average of 91%. The two-cycle residual amplifier presents more problems of convergence and fault reflection.

Besides that, so as to develop the complete test of the ADC, it is necessary to use two different designs for the sensor, since the configuration of the sensor is not equal for testing switched current cells than opamps, although both are based on the same detection methodology.

Finally, in the two topologies, the use our dynamic sensor, connected first to the last current copier of the conversion cycle and, after that, to the comparison circuitry, permits a fault coverage of 94% of the simulated faults, both in the SI and S^2I structures.

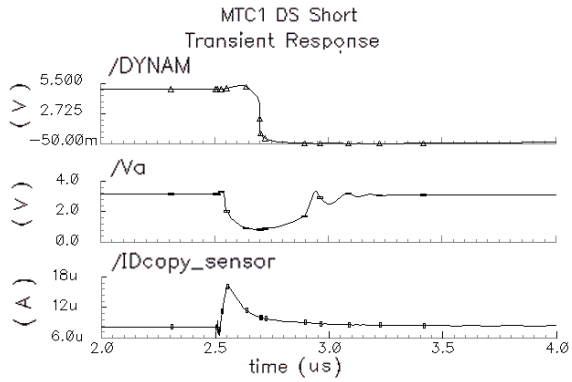

Figure 12. Output of the dynamic sensor in an example of faulty case.

An example of fault detection for this ADC can be seen in Figure 12, where this detection has been done by the slope sensitive stage of our sensor. It is the case of a Drain-Source short in the cascode transistor of the fine memory in the third current copier of the converter.

7. CONCLUSIONS

This paper presents the application of a test approach based on the analysis of the dynamic power supply current to algorithmic A/D Converters.

Two algorithmic A/D structures have been studied, with different topologies of current cells for each of them: basic SI, S^2I and fully differential.

An additional algorithmic A/D SC structures have been studied with a different charge detection sensor to compare the previous results of the algorithmic SI analog to digital converters with the SC circuit.

In all the A/D Converters we propose the use of Built-in Sensor in order to sample the current transients or the charge of the CUT. This use has permitted the development of a go/no go test that detects the presence of a fault in switched current and SC algorithmic A/D Converters.

The current sensor has been designed with the aim of prioritising the information obtained from the higher frequency components of the current over the information provided by quiescent current. For this reason an inductance has been implemented as a loading element of the current to

voltage conversion circuit. In the other side the charse sensor actually is an standard version that will be improved as a future work

Simulation test results have been obtained in order to prove the validity of this test approach for fault detection in this kind of A/D Converters based on switched-current and SC architectures, with good results.

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