DESIGN CONSIDERATIONS FOR SD MODULATORS BEYOND ADSL

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ABSTRACT

In this paper we discuss design considerations for Sigma-Delta modulators (ΣΔM) aimed at high-linearity, high-speed A/D conversion, as required in emerging wireline access applications. In order to achieve resolutions in the range 12-15bit with sufficiently low oversampling ratio, we analyze the performance of a family of high-order cascade multi-bit architectures in a low-voltage, deep-submicron scenario. We show that, after proper architecture selection, guided by a simple power estimation method, these ΣΔMs are still promising candidates to achieve post-ADSL performances in coming CMOS processes.

En este artículo se tratan consideraciones de diseño de moduladores Sigma-Delta (ΣΔM) para la conversión A/D de alta linealidad y frecuencia, tal como se requiere en las nuevas aplicaciones de acceso por cable. Con el fin de obtener resoluciones en el rango 12 a 15 bits con una razón de sobremuestreo suficientemente baja, se analizan las prestaciones de una familia de arquitecturas de alto orden en cascada con cuantización multibit, todo ello en el contexto de tecnologías profundamente submicrométricas con baja tensión de alimentación. Se demuestra que, tras una selección adecuada de la arquitectura, soportada por un procedimiento sencillo para la estimación del consumo de potencia, estos ΣΔMs resultan prometedores para alcanzar prestaciones post-ADSL en los futuros procesos CMOS.

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In this paper we discuss design considerations for Sigma-Delta modulators (ΣΔM) aimed at high-linearity, high-speed A/D conversion, as required in emerging wireline access applications. In order to achieve resolutions in the range 12-15bit with sufficiently low oversampling ratio, we analyze the performance of a family of high-order cascade multi-bit architectures in a low-voltage, deep-submicron scenario. We show that, after proper architecture selection, guided by a simple power estimation method, these ΣΔMs are still promising candidates to achieve post-ADSL performances in coming CMOS processes.

1. INTRODUCTION

Supported by a considerable commercial success, wireline solutions for broadband access or home networking are evolving to provide ever increasing data-rates and more functionality. Present ADSL is an example of such applications and extensions of this technology like ADSL+ (with doubled number of channels) or VDSL (providing video-rate reception) are just round the corner. As this trend goes on, the demand for highly linear, fast analog front-ends challenges mixed-signal designers to find converter architectures able to provide 12-15bit accuracy for signal bandwidths ranging from 1.1 to 12MHz [1].

Although these specifications seem a priori better suited for Nyquist architectures, such as a pipeline ADC, they do not exhibit enough linearity for some modulation techniques, specially in low-voltage implementations. For this reason oversampled A/D converters have gained ground in this frequency range. Specifically, sigma-delta modulators (ΣΔM) [2] exhibit high linearity making use of relatively simple circuitry, which render them worth exploring for the implementation of wireline modems as mixed-signal systems on-chip.

However, given the high signal bandwidths required in wireline communication, only low-oversampling ΣΔMs are feasible. This means a serious handicap, because as the oversampling ratio (M) decreases, some of their good properties vanish into thin air. In fact, low-oversampling modulators have an increased analog content (sometimes prone to instability [2]), and are more sensitive to errors, such as circuit noise, non-linearity, leakage, mismatching, etc. [2][3]. All things considered, a careful mixed-signal design is mandatory in order to compete with the Nyquist approach.

This paper discusses both architecture and design considerations for high bandwidth ΣΔMs for wireline applications beyond ADSL and in a deep-submicron CMOS context. Section 2 is aimed at searching for ΣΔM architectures compatible with low oversampling ratio. Also in this section, the impact of the main non-ideal mechanisms is revised. In section 3, after introducing a simple power estimation method, the architectures above are compared from the practical implementation point of view, and conclusions are drawn in section 4.

2. LOW-OVERSAMPLING SD MODULATORS

The oversampling ratio largely influences the performance of a ΣΔM, but there are two other important design parameters, namely: the modulator order (L) and the resolution of the internal quantizer (B) – see Fig.1. By using additive-error, linearized models [2][3], simple z-domain algebra shows that, under ideal operating conditions, the dynamic range (DR) of a ΣΔM is given by:

$$DR_{dB} = 10\log\left[\frac{3}{2}(2^B-1)^2\frac{(2L+1)\cdot M^{2L+1}}{\pi^{2L}}\right] \qquad ENOB = \frac{DR_{dB}-1.76}{6.02} \tag{1}$$

In order to avoid infeasible sampling frequencies, M cannot be too large in a broadband ΣΔM. So, high-order filtering (increasing L) and/or multi-bit quantization ($B>1$) must be employed for obtaining the required resolution.

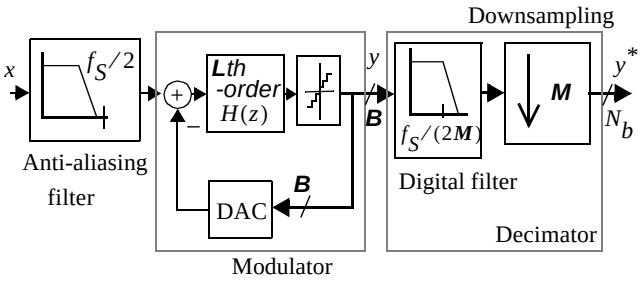

Figure 1. Block diagram of a ΣΔ A/D converter.

Both solutions decrease the original robustness of the highly-oversampled low-order single-bit ΣΔ conversion. For example, high-order ΣΔ loops are prone to instability, and the stabilization methods proposed have resulted in complex architectures whose dynamic range is seriously degraded with respect to that predicted by eq. (1) [2]. On the other hand, multi-bit conversion entails extreme sensitivity to the non-linearity of the DAC in the feedback path (see Fig.1) that must be calibrated [4]-[6]. However, since DACs cannot be efficiently linearized within an arbitrarily large resolution, the use of low-order multi-bit modulation may not be enough to obtain a given *DR*. A direct solution to this problem is to increase both the modulator order and the internal quantization resolution, giving rise to moderate-order (3-5), multi-bit architectures. In fact, the use of multi-bit quantization in single-loop high-order modulators inherently improves their stability properties [2], so that these are good candidates to obtain high-resolution, high-frequency operation, provided that the non-linearity problem is solved [4].

2.1 Expandible cascade multi-bit architecture

With the same objective, the combination of high-order cascade (MASH) architectures with multi-bit quantization has been proposed [3][7]-[9]. These modulators gather the unconditional stability of cascade modulators (provided that only second- and/or first-order stages are used) and the advantages of multi-bit quantization with relaxed requirements for the linearity of the latter. The feasibility and efficiency of this approach, because it needs no correction/calibration mechanism, has been proved in analog technologies [3][7][10].

Further investigation into the potentialities of these architectures have led us to propose an easily expandible, modular family of high-order cascades. Fig.2 shows the block diagram of a generic element of such a family. It is a *L*th-order modulator formed by a second-order stage followed by $L-2$ identical first-order stages (2-1^{L-2} ΣΔM). The values of their integrator weights are:

$$g_{1a} = g_{1a}' = 0.25 \qquad g_{1b} = 1, g_{1b}' = 0.5$$
$$g_k = 1, g_k' = 0.5, g_k'' = 0.5 \qquad k = 2, \ldots, L-1 \tag{2}$$

The outputs of the $L-1$ stages are combined in the digital domain by simple operators, $H_k(z) = (1-z^{-1})^k$, to cancel out the quantization noise generated in each stage but the last one. Additionally, a pseudo-multibit operation is achieved by including multi-bit quantization only in the last stage, while the remaining are single-bit. Linearized z-domain analysis shows that the modulator output can be expressed as follows:

$$Y(z) = z^{-L} \cdot X(z) + 2(1-z^{-1})^L \cdot E_N(z) + 2(1-z^{-1})^{(L-L_N)} \cdot E_{INL}(z) \tag{3}$$

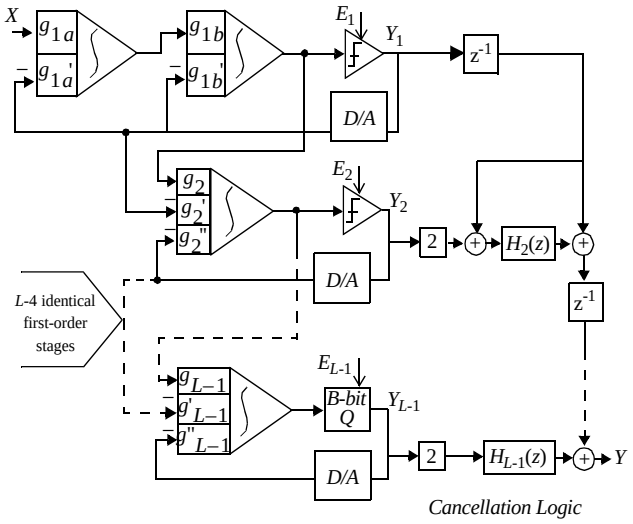

Figure 2. *L*th-order ΣΔ modulator using a 2-1^{L-2} cascade.

where $X(z)$ stands for the input signal, which is simply delayed, $E_N(z)$ is the last-stage quantization error, which is shaped by a *L*th-order function, and $E_{INL}(z)$ represents the non-linearity error of the last-stage DAC. Note that since $E_N(z)$ is generated in a B-bit quantizer, the modulator response equals that of an ideal L th-order B-bit ΣΔM, except for the factor 2. The aim of this factor, that equals $g''_{L-1}/(g'_{1a}g_{1b}g_2 \cdots g_{L-1})$, is to compensate for the signal scaling required to avoid premature overloading of the modulator. Since this factor also amplifies the last-stage quantization error, a systematic loss of resolution is always found in cascade ΣΔMs. However, with the coefficients given in (2) this loss is reduced to 1b (or 6dB *DR*), one of the lowest achievable. More importantly, this factor is constant, regardless of the number of stages. In fact, the most appealing feature of this architecture (with the set of coefficients proposed) is that it can be easily set to any order just by changing the number of identical first-order stages. As shown in Fig.3, a correct operation is maintained with constant overloading point, no matter how high the overall order is.

The set of coefficients in (2) also has the following interesting properties: (a) The total output swing (*OS*) required in all integrators is reduced to only the quantizer full-scale. (b) By proper sharing of the SC input stages, they can be implemented with just two-branch integrators, which also minimizes the number of unitary capacitors. (c) All first-order stages, but the last one in case of using multi-bit quantization, contain the same analog and digital coefficients, and they can be electrically identical as well. This considerably simplifies the electrical and physical implementation of the converter.

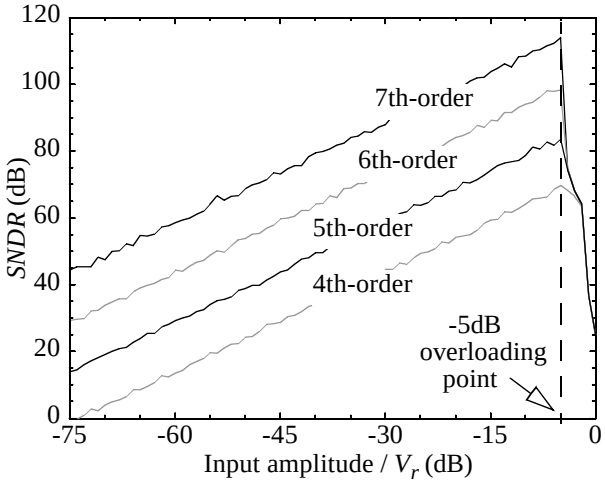

Figure 3. *SNDR* vs. the input level for several modulator orders. Note that the overloading point does not change from curve to curve.

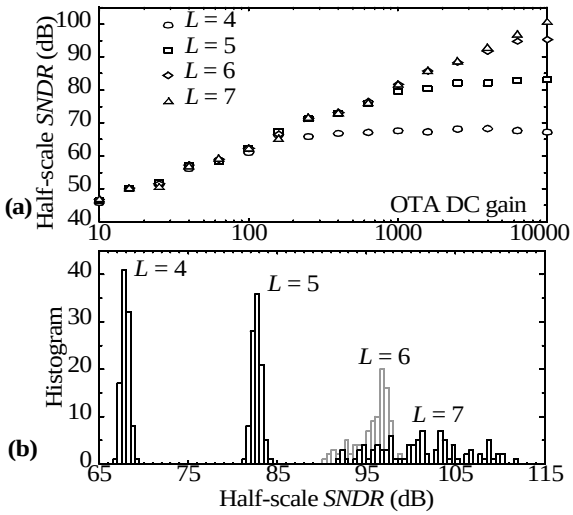

Figure 4. Effect of (a) finite DC-gain and (b) weight mismatch on the *SNDR* of single-bit 2-1^{L-2}ΣΔMs for $M = 16$.

2.2 Non-ideal performance

Switched-capacitor implementations of cascade modulators suffer from certain non-ideal behaviors more than their single-loop counterparts, namely: finite (and non-linear) OTA DC-gain and capacitor mismatching [3]. Both non-idealities modify the ideal integrator z-domain transfer function, thus altering the quantization error transfer function. Since the cancellation logic is not changed, mismatching appears between the analog and digital processing that precludes perfect cancellation of the low-order quantization error. For certain levels of DC-gain and capacitor mismatching, this leakage of quantization error may mask the ideal contribution, thus imposing an upper bound to the practical values of L.

In order to estimate this limit under realistic circuit imperfections, Fig.4(a) shows the simulated half-scale *SNDR* as a function of the OTA DC-gain for $M = 16$. Fig.4(b) shows the *SNDR* histograms obtained from MonteCarlo simulation assuming 0.1% sigma in capacitor ratios (0.05% is currently featured by metal-insulator-metal capacitors in CMOS processes [11]). Under these conditions, mainly because of the matching sensitivity, the 7th-order architecture is not worth implementing. Nevertheless, the 6th-order modulator provides 90dB worst-case *SNDR* with DC-gain of 2500. Especially robust is the 5th-order cascade requiring a DC-gain of 1000 to achieve 80dB worst-case *SNDR* with $M = 16$. It is important to remark that these gains are basically needed for the first-stage OTAs. The DC-gain requirement for the integrators in the remaining $L - 2$ stages of the cascade can be relaxed. This is also applicable to other circuit imperfections such us noise, finite dynamics, non-linearity, mismatching, etc. This practice allows us to use simpler circuits and layouts for these stages, thus saving area and power consumption.

In the same way, in practice the number of bits in the last-stage quantizer cannot be arbitrarily large. As shown in Fig.5, for a given oversampling ratio, the evolution of the effective resolution with B tends to saturate due to the presence of leakage. Nevertheless, depending on the signal bandwidth, the reduction in oversampling ratio that can be achieved by resorting to multi-bit quantization may define the border between feasible and infeasible implementations. As we will show further on, proper selection of the three main design parameters (L, M, and B) is the key to really efficient implementations.

3. DEEP-SUBMICRON DESIGN CONSIDERATIONS

Viability of cascade multi-bit architectures in deep-submicron CMOS processes is mainly related to: (a) supply voltage and (b) capacitor performance.

The supply voltage, through the selection of the reference voltages, defines the available dynamic range, but it

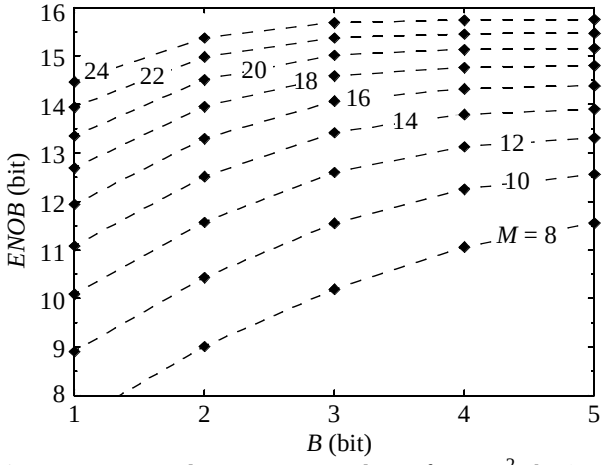

Figure 5. *ENOB* vs. last-quantizer resolution for a 2-1^2mb ΣΔM in the presence of circuit imperfections.

also makes an impact on the selection of the OTA topology. In fact, two-stage topologies are required for some integrators in the cascade modulator for implementations in processes with 3.3-V supply and below. Definitely, this will be the choice from now on.

Apart from the OTAs, the performance of the switches with supply voltages below 2.5V needs careful control, especially for dynamic distortion considerations. A solution is found in the clock-boosting strategies, with the subsequent increase in circuit complexity and power dissipation. Another solution to this problem could be using higher voltage devices in those processes with double oxide thickness. For now, when available, such devices are often poorly modeled for signal processing. Low-VT devices are also optionally available in modern technologies, but at a higher price.

The second most relevant technology feature has to do with the quality of the capacitor structures. It has been shown that the capacitor matching requirements are in the range of 0.1% - 0.2% standard deviation. Low parasitics are also of extreme importance for an efficient implementation of a high-frequency modulator. Finally, we have the capacitor linearity requirements, which are less demanding provided that matched fully-differential circuitry is used. Fortunately, metal-insulator-metal (M-i-M) capacitor structures are now available in CMOS processes [11]. They exhibit an excellent matching and linearity, with very small bottom parasitics. If these capacitors are to be available in the coming CMOS technology, they will not contribute any loss of performance.

In order to quantitatively evaluate the previous assumptions, we will develop an analytical procedure to roughly estimate the power consumption of different cascade single-bit and/or multi-bit sigma-delta modulators. In these expressions, both architecture and technological features will be contemplated, together with simplifying assumptions inspired in practical design solutions. The aim is not only to draw conclusions about architectural choices, but also to track their evolution under technology changes.

3.1 Dominant error mechanisms in high-frequency ΣΔ modulators

In the presence of circuit imperfections, the dynamic range (*DR*) of a ΣΔM can be roughly expressed as follows,

$$DR = 3 \cdot 2^{2ENOB-1} \cong \frac{V_r^2/2}{P_Q + P_{Th} + P_{St}} \qquad (4)$$

where V_r represents the full-scale input range of the modulator (which equals the reference voltage) and P_Q, P_{Th}, and P_{St} are the in-band powers of the quantization error, thermal noise, and incomplete settling error, respectively. An equilibrium among them, so that $P_Q \approx P_{Th} + P_{St}$, is behind all well-designed ΣΔMs.

Note from (4) that increasing V_r has a valuable effect on resolution. However, it is obviously constrained by the supply voltage. The clearest reasoning is that the output swing requirement in integrators for a given V_r must be feasible in the technology considered. Thus, the selection of V_r is closely related to the type of OTA forming the integrator and its capability to trade open-loop DC-gain, speed and output swing [12][13]. An empirical upper bound for a feasible selection of V_r is given by:

$$V_r = V_{\text{supply}} - n_{ob} V_{sat}, \text{ in volt-peak differential,} \qquad (5)$$

where V_{sat} is the saturation voltage of the output devices and n_{ob} is the number of transistors in the output branch, which again depends on the specific OTA topology. For the sake of simplicity, we will assume that cascode devices will be used in single-stage OTAs. This means that our single-stage OTA will be the popular folded-cascode OTA, with $n_{ob} = 4$. However, as stated before, this common choice is not always enough to achieve a good DC-gain, output swing trade-off. This is specially true for low-voltage implementations, where an excessive value of V_{sat} will result in a ridiculously small value for the feasible reference voltage, thus producing little efficient modulators. Among the alternatives, we count on two-stage OTAs [12][13], whose output branch can contain only two transistors ($n_{ob} = 2$) still producing a large open-loop DC gain. This allows us to increase the value of the reference voltage up to useful levels.

For the sake of simplicity, we will assume for now that the incomplete settling error can be controlled by design so that $P_{St} \ll P_Q, P_{Th}$. With respect to P_Q, it is formed by three main error mechanisms: (a) last-stage quantization error; (b) last-stage DAC non-linearity (for multi-bit quantization only); and (c) non-cancelled portion of the low-order quantization errors caused by leakage. A close expression, including all these non-idealities is

$$P_Q = \sigma_{mQ}^2 d^2 \frac{\pi^{2L}}{(2L+1)M^{2L+1}} + \sigma_{INL}^2 d^2 \frac{\pi^{2(L-1)}}{(2L-1)M^{2L-1}} + \sigma_{sQ}^2 \left(\frac{25}{48} \frac{\pi^2}{A_v^2 M^3} + 24\sigma_C^2 \frac{\pi^4}{5M^5} \right) \qquad (6)$$

where the three contributions above are included, with A_v being the first-stage OTA DC-gain, σ_C the capacitor mismatching standard deviation, and

$$\sigma_{mQ}^2 = \left(\frac{2V_r}{2^B - 1} \right)^2 / 12 \qquad \sigma_{INL}^2 = \frac{(2V_r \times INL)^2}{2} \qquad \sigma_{sQ}^2 = \frac{(2V_r)^2}{12} \qquad (7)$$

are the total powers of errors (a), (b), and (c), respectively.

Concerning P_{Th}, it will be usually dominated by white noise. Other noise sources, such as $1/f$ noise, are intended

for playing a secondary role, the reason being twofold: (a) DC and the low-frequency region of the spectrum are normally out of the signal band in telecom applications; (b) the usage of small capacitors in order to relax the dynamic requirements increases kT/C noise over the flicker noise components. A conservative expression for the in-band power of thermal white noise can be derived [3],

$$P_{Th} \cong \frac{16kT}{3MC_s} \tag{8}$$

where C_s is the value of the sampling capacitor.

3.2 Estimation of the power consumption

Previous equations show that the dynamic range of a cascade ΣΔM can be roughly expressed as a function of the following design parameters: V_{supply}, L, M, C_s, A_v, and σ_C, to which we have to add B and INL if the last-stage quantizer is multi-bit. So, for given values of A_v, σ_C, and INL, the minimum value of the capacitor C_s required to obtain a given DR can be obtained as a function of M, L, and B. Once C_s is known, the equivalent load for the OTA in the integrator can be estimated as,

$$C_{eq} \cong C_s + C_p + C_l\left(1 + \frac{C_s + C_p}{C_o}\right) \tag{9}$$

where C_o, the integrator feedback capacitance, is related to C_s through the integrator weight, $C_o = C_s/g_i$; and C_p, C_l stand for the integrator summing node and output parasitics, respectively. Estimating the latter two capacitances is a difficult task because of their extreme dependence on the actual OTA design.

Usually, the main contribution to C_p is the OTA input parasitics. In a fully-differential topology, this is formed by the input transistor gate-to-source capacitance C_{gs} (both channel and overlap contributions) and its overlap gate-to-drain capacitance C_{gd}^{ov} amplified by Miller effect. Thus, neglecting C_{gb},

$$C_p \cong C_{gs}^{\text{ch}} + C_{gs}^{\text{ov}} + C_{gd}^{\text{ov}}(1 + A_{v_1}) = \frac{2}{3}C_{ox}'W_{in}L_{in} + C_{ox}'W_{in}\Delta L_{in}(A_{v_1} + 2) \tag{10}$$

where C_{ox}' is the gate oxide capacitance density, and ΔL_{in} stands for the lateral diffusion of drain/source regions below the gate, both technology-dependent parameters. Apart from the input transistor dimensions W_{in}, L_{in}, the other unknown variable in eq. (10) is its input-to-output gain A_{v_1}. This is equal to the complete gain of the OTA for single-stage amplifiers, or to the first-stage gain if multi-stage topologies are used. It can even be around unity if cascode devices are used, such as in folded- or telescope-cascode OTAs [12][13]. Now, making use of the well-known (as much as inadequate) square-low expression for the input transistor drain current,

$$C_p = \frac{2L_{in}I_{D,in}}{\mu V_{OVD}^2}\left[\frac{2}{3}L_{in} + \Delta L_{in}(A_{v_1} + 2)\right] \tag{11}$$

where $V_{OVD} \equiv V_{GS} - V_T$ is the input transistor overdrive voltage.

The other unknown capacitance in (9), C_l has two main contributions: the first one is due to the bottom parasitic of the integration capacitor C_o, and the second one is due to the OTA itself. The former contribution can vary a lot, depending on the type of capacitors. With modern M-i-M structures it turns out to be very small, ranging from less than 1% to 5% of C_o. Because of this, C_l tends to be dominated by the OTA output parasitic load, which strongly depends on the actual output devices and, overall, the OTA topology. Even the supply voltage, via output swing and DC-gain requirements, makes an impact on the transistor sizes and hence on C_l. For a given OTA schematic, the latter influence makes C_l slightly increase under technology scaling and shrinking supply voltages, because wider output devices are required to accommodate similar output swings. All things considered, a reliable estimation of this capacitance prior to sizing the OTA is not possible. Based on previous design experiences, we will assume a constant value equal to 2.5pF.

Let us return to the settling error power, P_{St}. An accurate estimation of the settling error would involve the following calculations. For example, just for a single-pole OTA model, complicate expressions are derived [3] if a non-linear (slew-rate limited) settling is considered. Further complexity arises from considering both sampling and integration incomplete charge-transference and the contribution of the non-zero switch on-resistance [14]. Hence, we will simplify our treatment assuming that the slew-rate of the OTA is large enough and the switch on-resistance small enough to neglect their impact on the integrator transient response, so that the settling is linear with time constant equal to C_{eq}/g_m. This being the case, it takes a number $\ln(2^{ENOB})$ of time constants to settle within $ENOB$ resolution; that is, the following relation should be fulfilled:

$$\ln[2^{(ENOB+1)}]C_{eq}/g_m \le T_S/2 \tag{12}$$

where T_S is the sampling period. Note that we have added an extra bit in order to make room for the inaccuracy of this simplified model. The above expression can be used to estimate the minimum value of the transconductance parameter as,

$$g_m = 2f_S\ln[2^{(ENOB+1)}]C_{eq} \tag{13}$$

where $f_S \equiv 1/T_S$ is the sampling frequency. This is the transconductance required for a single-stage OTA, for which C_{eq} in eq. (9) is the equivalent output load. For multi-stage OTAs, the previous relation must be carefully tackled because both parameters, total transconductance and

equivalent output load, lose control of the amplifier dynamics. However, provided that the main pole of the OTA is set by the input stage and an eventual inter-stage compensation capacitor, eq. (13) can still be used to determine the input stage transconductance that is related to the input transistor current as follows

$$g_m = \frac{2I_{D,in}}{V_{OVD}} \tag{14}$$

Equations (9), (11), (13), and (14) can be handled in an iterative manner to determine the current required through the input transistors of the OTA, whose actual topology sets the power consumption. Fig.6 shows several OTA schematics including both single- and two-stage topologies. Whenever possible, a single-stage OTAs should be used for its better performance/power figure. However, as discussed previously, as technologies scale down and supply voltages shrink, two-stage OTAs are gaining ground. Moreover, in practice two gain stages are not enough to achieve the overall gain requirement, so that the first one often includes cascode devices in a telescope cascode configuration like in Fig.6(b) and (c).

Let's consider this topology as an archetype in modern deep submicron technologies. The current through the first stage has been already estimated as $2I_{D,in}$. Assuming for the sake of simplicity a fixed ratio η_{io} between the currents flowing through the input and output branches, the total current through the OTA can be estimated as,

$$I_B \cong 2I_{D,in} + 2\eta_{io}I_{D,in} + I_{D,in} = [2(1+\eta_{io}) + 1]I_{D,in} \tag{15}$$

where an extra $I_{D,in}$ has been added to account for the current used in the OTA biasing stage.

With eq. (15) the power dissipation of the first OTA can be estimated. That of the remaining OTAs in the cascade stages can be decreased with respect to the former, following the scaling rule commonly applied to the amplifier requirements in ΣΔMs. This power reduction may come from either a relaxed set of specifications, or the subsequent amplifier topology simplification. Sometimes, even when a two-stage OTA may be required for the first integrator, it is possible to use a single-stage topology for the second and successive integrators. So, we can write

$$I_{B,total} = I_B\left(1 + \sum_{i=2}^{L}\chi_i\right) \tag{16}$$

where χ_i is the ratio between the current absorption of the *i*-th OTA and the first one. From this, the static power dissipated in the OTAs amounts to,

$$P_{op,\,sta} = I_B V_{supply}\left(1 + \sum_{i=2}^{L}\chi_i\right) \tag{17}$$

Apart from the static consumption in the OTAs, which usually accounts for 80% of the total power, there are other contributing blocks, namely:

- $L-1$ latched comparators used as single-bit quantizers, and those forming the last-stage multi-bit quantizers, usually implemented by a flash A/D converter, i.e. (2^B-1) more latches. This consumption must include the static power dissipated in a convenient pre-amplifying stage (see Fig.7).
- Last-stage multi-bit DAC (if $B>1$). The relaxed requirements for this block allows us to implemented it with a resistor ladder. Its main design considerations are resistor matching and linearity (both causing *INL*), and the fact that it must drive enough current to provide a good settling. The current requirement scales with the sampling frequency and the capacitive load involved. The latter can be considered almost constant because the last-stage capacitors should be set to the minimum required to achieve certain level of matching (thermal noise playing a secondary role). So, we can empirically write:

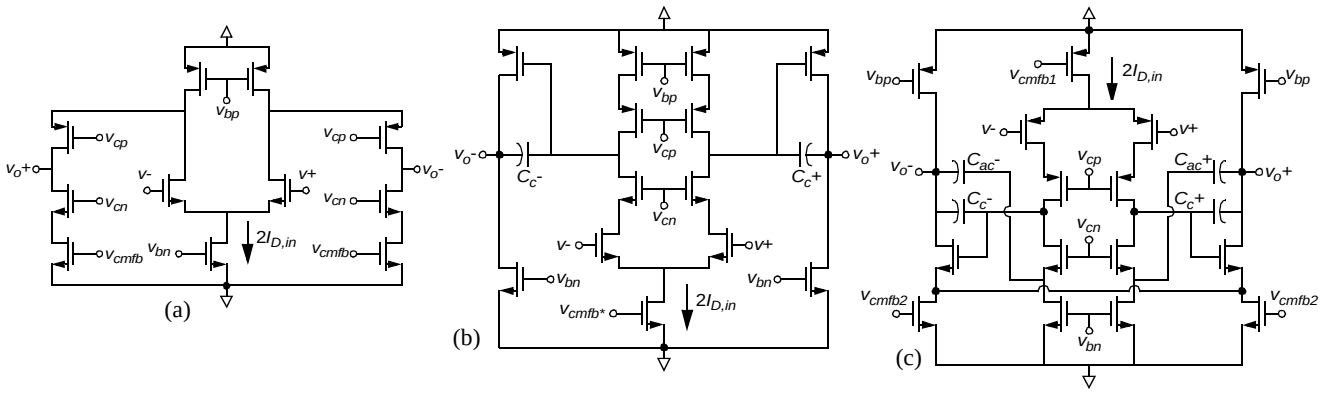

Figure 6. Three possible fully-differential OTA topologies: (a) Single-stage folded-cascode OTA; (b) Two-stage Miller compensated OTA with telescope-cascode first stage; (c) Two-stage two-path compensated OTA with telescope-cascode first stage and differential pair-based second stage.

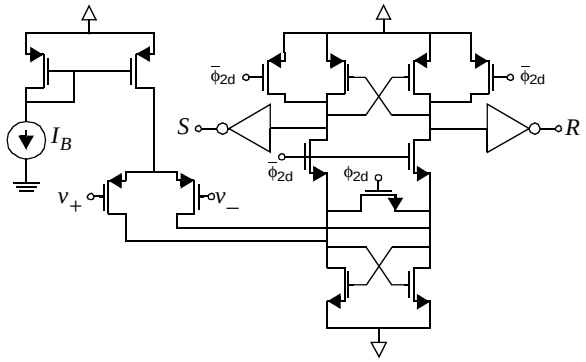

Figure 7. Pre-amplifying, latched comparator with a differential pair as input transconductor.

$$P_{DAC} \cong V_{\text{supply}} I_{DAC,\,\text{ref}} \times \frac{f_S}{f_{S,\,\text{ref}}} \tag{18}$$

where $I_{DAC,\,\text{ref}}$ is the current through the resistor ladder DAC required for operating at a certain frequency of reference, $f_{S,\,\text{ref}}$.

- Dynamic power in SC stages. The dynamic power dissipated to switch a capacitance C_u between the reference voltages at a frequency f_S can be estimated as $C_u f_S V_r^2$, which tends to increase in high-speed, high-resolution converters. Its actual value depends on the integrator weights used. In our case, the following expression provides a good estimate:

$$P_{SC} = 2 \times [5C_{u_1} + 4(L-1)C_{u_2}] f_S V_r^2 \tag{19}$$

where the factor 2 comes from the differential implementation; C_{u_1} is the unitary capacitor used in the first integrator, whereas C_{u_2} is the one used in the second and following integrators, usually smaller than C_{u_1}.

- Small digital blocks: flip-flops, gates, cancellation logic, etc. Apart from being small, they do not make any difference for the architectures considered, and will be neglected here. Of course, this does not apply to the decimation filter, whose power consumption is comparable to that of the modulator. Moreover, since the order of the digital filter must equal $L + 1$, high-order ΣΔMs require more complex filters than low-order ones. However, an increase of the modulator order entails a decrease of the oversampling ratio, the filter can be operated at a lower frequency and dissipates less power. To our purpose, we can consider an essentially constant decimation filter power consumption.

By adding up all the contributions, the power dissipation of the ΣΔM can be estimated by,

$$P_{sta} \cong P_{op,\,\text{sta}} + \\ + P_{DAC} + [(L-1) + (2^B - 1)] P_{comp} + P_{SC} \tag{20}$$

3.3 Comparison among cascade architectures

In this section we make use of the power estimate to compare several cascade ΣΔMs in the presence of both specification and technology changes. To this end, the following figure-of-merit (*FOM*) has been used,

$$FOM = \frac{Power}{2^{\text{ENOB}} \times DOR} \times 10^{12} \tag{21}$$

where *DOR* stands for the digital output rate, i.e., the Nyquist rate.

In a first comparison step, the triads {*L, M, B*} describing a specific cascade have been evaluated along the curve in the resolution–speed plane shown in Fig.8 (dashed line). Although this particular resolution–speed relationship is arbitrary, it fits the usual requirements for wireline telecom ADCs: ISDN, ADSL, VDSL, etc., which have been placed in the figure for illustration. For each section of the resolution–speed curve, the architecture with the minimum *FOM* has been noted down. Observe that the oversampling ratio decreases as the output rate increases and, simultaneously, the multi-bit quantization shows up to compensate for the oversampling reduction.

In a second step, we take advantage of the fact that some technology features enter the above formulation to predict how the performance of the cascade ΣΔMs is going to evolve under technology changes. Fig.9 shows the estimated evolution of the *FOM* of three cascade topologies, namely {4, 24, 1}, {5, 16, 1.5} and {4, 16, 3}, aimed at obtaining 14bit at 4.4MS/s. These are typical specifications for ADSL+ modems. Two facts are noticeable:

- Despite the reduction of the supply voltage, overall, the power dissipation does not decrease below 0.18μm. This is basically due to the reduction in supply voltages, which imposes a reduction in the reference voltage and, hence, the signal power. In order to keep the effective resolution,

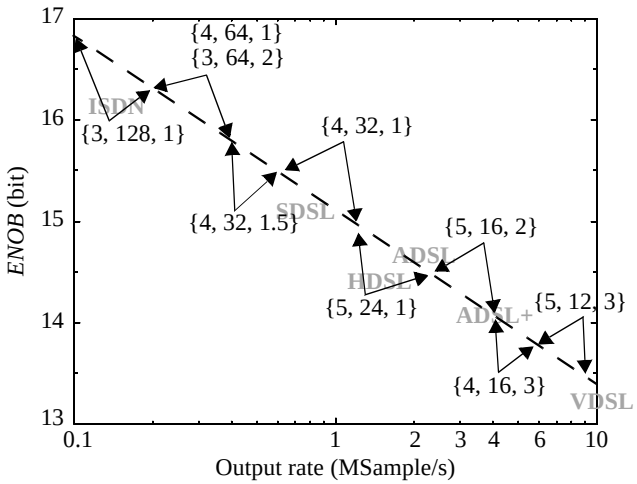

Figure 8. Most efficient cascade ΣΔM for each region of the resolution - speed plane.

this loss of signal power must be compensated by an equivalent reduction of the noise power, which can be achieved by increasing the value of the sampling capacitors. Since the incomplete settling error power must be also kept constant, the larger the capacitances, the more demanding the dynamic requirements for the OTAs. Whereas up to 0.18μm the increase in current absorption caused by this mechanism is compensated, in terms of power, by the supply voltage scaling, the estimated trend is exactly the opposite below that technology. Once again, the location of the inflection point depends on the converter specifications. For instance, if for the same speed, the resolution is to be increased, the inflection point moves to the right in Fig.9.

- Another aspect illustrated in Fig.9 is the dynamic nature of the architecture selection in Fig.8. Note the evolution of the {4, 16, 3} ΣΔM. It outperforms for 0.25μm and above, but it does not below 0.18μm. The reason behind this is that the multi-bit modulator has a fixed amount of power contributed by the last-stage quantizer that is not present in the single-bit implementation ({4, 24, 1} ΣΔM). In addition, the latter takes advantage of the faster technologies to compensate for the increased oversampling ratio with respect to the multi-bit modulator. The fifth-order {5, 16, 1.5} ΣΔM deserves especial attention. If the quality of the M-i-M capacitors is preserved, this architecture will be worth exploring in the coming technologies.

4. CONCLUSIONS

We have analyzed the performance of family of cascade multi-bit ΣΔMs in a deep-submicron context. Design considerations comprising architecture, electrical implementation, and fabrication process issues have been discussed. In doing so, a simple but effective power estimate has been derived, useful for architecture exploration against specification and process changes. It has been shown that, after proper architecture selection, the ΣΔMs here are good candidates for achieving the specifications currently demanded by most extended wireline access technologies. In addition, although process scaling will preclude further power reduction, our conclusion is that some cascade multi-bit ΣΔMs will be worth exploring in 0.13μm and below.

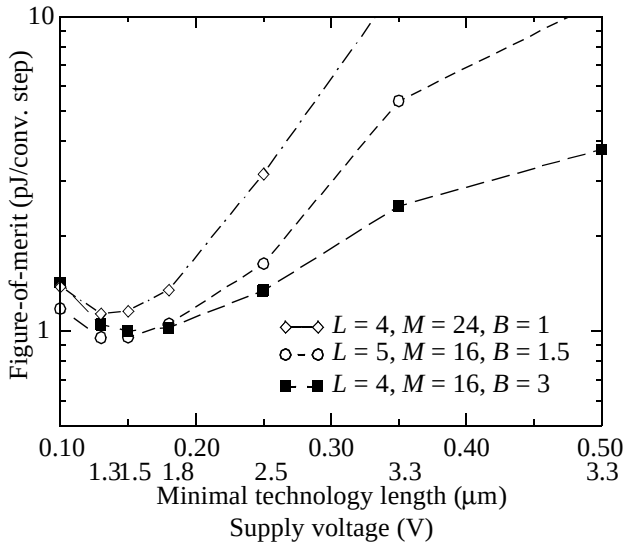

Figure 9. Estimated evolution of the *FOM* with technology for three cascade architectures obtaining 14bit@4.4MS/s.

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