CONTROLLING EMC PERFOMANCE IN INTEGRATED CIRCUITS. A CONDUCTED IMMUNITY TEST METHOD.

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ABSTRACT

Due to increasing demands for electromagnetic immunity on chip-level in combination with more complex circuits and faster design cycles, it is mandatory to spend effort on achieving electromagnetic compatibility (EMC) at this level.

This paper deals with the susceptibility of integrated circuits (IC) to voltage dips, voltage interruptions and variations, and ripple on the Vcc/Gng processor power lines.

It presents a measurement method to evaluate electromagnetic immunity of Integrated circuits based on the Standards IEC 671000-4-29 and IEC 61000-4-17, on a MSP430-1 Texas microcontroller board, used as set-up for the test.

It presents the evaluation of the effectiveness of some classical SW-based fault detection mechanisms for conducted EMI-induced faults.

(*) *Members of "Red Pucara" CYTED IX.G, Red Iberoamericana de Certificación y Calificación de Componentes y Sistemas Microelectrónicos*

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1. INTRODUCTION

The widespread use of small, high speed electronic devices which are often operated near other electrical systems, as well as the explosion in the number and variety of wireless communication devices available, has resulted in concern about interference effects. Faster and more complex circuits are being crowded into ever smaller spaces, increasing the likelihood that devices containing such systems will adversely affect one another. Modern electronic devices must therefore be able function properly in an increasingly cluttered electromagnetic environment.

Often the effects of electromagnetic interference are not discovered until product testing occurs. The resolution of interference problems in the late phases of product development often involves the addition of "extraneous" components, which add to system complexity, reduce reliability and make the product more expensive.

Additionally, it is illegal to sell products, which do not meet government regulations and Directives regarding electromagnetic emissions; especially in USA and Europe. It is therefore desirable that electromagnetic interference issues, and compliance with International Regulations regarding emissions and susceptibility, be addressed in the initial stages of product design.

Then, there are obvious benefits to test and control Electromagnetic Interference (EMI) directly at the chip level through an appropriate test system.

For these reasons, systems must be designed not only to minimize emissions, but also to be immune from external interference. Unfortunately, as the

electromagnetic environment becomes more complex, this goal becomes more difficult to achieve.

Thus, the minimization of electromagnetic interference (EMI) and susceptibility (EMS) has become a major design objective.

2. CONDUCTED ELECTROMAGNETIC INTERFERENCE ON ELECTRONICS

In the presence of electromagnetic RF incident field (produced for example by the cellular phone transmitting antenna), cables connected to electronic systems and PCBs' tracks behave as receiving antennas capturing disturbances. The induced RF currents reach the inputs ports of ICs and often produce system malfunctioning [1].

In fact, the coupling effect between electromagnetic RF incident field and tracks routed on the die surface is lower than that one between electromagnetic (RF) incident field and PCB tracks connected to the input ports of an IC. In such a noisy environment, there are two types of failures induced by conducted RF interference on ICs [1]:

a) *Static failures*: occur in the presence of conducted RF interference superimposed on high or low logical level. The signal at the IC input port goes out of high or low noise margins. Sometimes, it can be observed synchronization between the input signal and the RF interference. In this case, errors at the IC's output ports come from failures in the IC input ports.

b) *Dynamic failures*: occur when conducted RF interference added to the IC input logical signal gives variation in the input port propagation delay. Thus, changing the logic gates settling time and hold time. In this case, errors due to conducted RF interference observed at the IC's output ports come from failures in internal sub-circuits.

The induced RF currents that reach the input ports of ICs may be caused from a simple voltage variation to a large voltage interruption in the IC power supply lines.

3. INTERNATIONAL STANDARDS APPLICABLE

Electromagnetic Interference (EMI) susceptibility of microprocessor-based systems is oriented according to international normatives. Some of them can be listed as: *International Standard IEC 61.000-4-29 and International Standard IEC 61.000-4-17* Normatives [2,3]. While the first one rules for testing proceedings for voltage dips, voltage interruptions, and voltage variations, the latter provides testing procedures for ripple on the Vcc/Gnd processor power lines.

Table I summarizes the types and time durations of the noise injected into the processor power lines according to the *International Standard IEC 61.000-4-29 Normative*.

Type of Disruption	Description: waveform and time duration	
Voltage Dips	a negative pulse of -30% of the Vcc power line	10ms
		100ms
		300ms
		X*
	a negative pulse of -60% of the Vcc power line	10ms
		100ms
		300ms
		X*
Short Interruptions	a negative pulse of -100% of the Vcc power line	10ms
		100ms
		300ms
		X*
Voltage Variations	a variation of –20% to +20% of the Vcc power line	continuous variation in the Vcc power line

- ***Open value(s) to be defined by the specific application or device to be tested.***

Table I. Summary of the *IEC 61.000-4-29 Normative* for voltage dips, short interruptions, and voltage variations.

4. DESCRIPTION OF THE CONDUCTED IMMUNITY TEST SET UP

Fig. 1 shows the test setup the research groups involved with "Red Pucará" **(CYTED** IX.G.-RED IBEROAMERICANA DE CERTIFICACIÓN Y CALIFICACIÓN DE COMPONENTES Y SISTEMAS MICROELECTRÓNICOS) have developed along the last months to inject electromagnetic-induced noise into the processor Vcc power line. This setup is organized around a *PC-based host*, whose goal is to serve as interface between the user and the device under test (*MSP430-1 Board*). This server communicates with the MSP430-1 via RS232 and JTAG (optic fiber) by one side and with the fault injection controller (or EMI Generator): *MSP430-2 Board*, by the other side. As can be seen in this figure, the program stored in the flash memory of the EMI Generator deals to control the *Driver Board* by means of sending control signals to the operational amplifier (Op Amp, in the Driver Board). Then, the Op Amp output is fed into a digital-to-analog converter (DAC), which in turn translates the digital voltage into an analog "noisy Vcc signal" in order to inject voltage dips into the MSP430-1 processor Vcc power pin (i.e., the device under test – DUT). The DUT in the MSP430-1 Board is a Texas Microcontroller MSP430F149 [4] which contains 60KB flash memory to store control program, and 2KB of RAM to store data as well as control state variable. This RAM also serves as stack area for the control part. Similarly, the MSP430-2 Board is also based on the same microcontroller device.

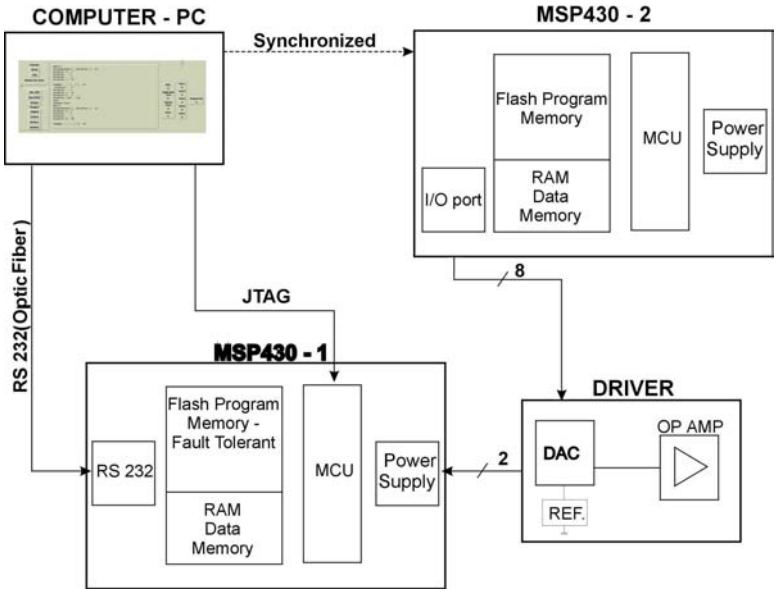

Fig. 1. Test setup used for electromagnetic-induced noise injection[1].

We have been evaluating the effectiveness of some classical SW-based fault detection mechanisms in detecting conducted EMI-induced faults. The main goal towards this evaluation process is to derive alternative low-cost approaches based on software implementations to improve systems robustness to EMI. The techniques implemented in software deal to detect two distinct types of faults: faults affecting data, and faults affecting the processor control-flow.

As one of our ongoing work, we will provide to the academia and industry communities the results involving the final robustness obtained by adding software-based fault-detection techniques in a system operating in EM-environment.

[1] There are several professional EMI generators commercially available in the international market. However, it should be noted that their typical prices could vary from two or three tens of thousands of dollars up to one hundred thousand dollars a unit. On the other hand, the test setup presented here is a simple, customized and economical conducted-EMI generator whose price turns around three thousand dollars a unit.

5. CONCLUSION

This paper deals with the characterization of integrated circuits (ICs) electromagnetic immunity. In particular, an assessment of IEC 61000-4-29 and IEC 61000-4-17 measurement procedure is presented.

This implementation tool will enable chip designers or manufacturers to run EMC tests for successive optimization of the floorplanning and power routing.

The proposed qualification scheme gives an easy way to qualify the IC and even the software.

Furthermore methods for testing of the susceptibility of integrated circuits against electromagnetic ware signals are under consideration.

10. REFERENCES

[1] Fiori, F.; Benelli, Gaidano, G.; Pozzolo, V. Investigation on VLSIs' Input Ports Susceptibility to Conduct RF Interference. IEEE Transactions on Electromagnetic Compatibility, 1997. pp.326-329.

[2] International Electrotechnical Commission - International Standard IEC 61000-4-17. (www.iec.ch)

[3] International Electrotechnical Commission - International Standard IEC 61000-4-29. (www.iec.ch)

[4] Microcontroller Texas MSP430F149. (www.ti.com)