

A simple FSK codec with built-in self-test and stand-by mode

Pablo Petrashin (1) – Eduardo Romero (2)

**(1) Universidad Católica de
Córdoba
Facultad de Ingeniería
Grupo de Microelectrónica
petra@uccor.edu.ar**

**(2) Universidad Tecnológica
Nacional de Villa María
Facultad de Ingeniería**

ABSTRACT

The present work deals with the design of a mixed analog - digital circuit for a FSK 1200 – 2400 Hz codec, using a stand alone oscillator as a reference clock. The circuit needs no crystal or any external components and includes a digital Built-in-selt-test (BIST) capability and a stand-by mode for low consumption. The self-test capability can not check the oscillator, although it is included in the test path. However, a brief study of two different methods for testing the oscillator is also presented. Finally, some simulation results and conclusions are shown, together with future work perspectives.

As a part of a major work oriented to interconnected sensors design, the need of digital communication using analog existing media (such as the power supply home network, analog telephony lines -twisted pairs-, etc) is permanently present. This kind of transmission requires the modulation of the digital information. A well-known standard format is the FSK (Frequency Shift Keying). The present idea is to achieve a design of a very simple, low consumption and robust circuit that could implement this codification, using standard CMOS technology. Robustness is assured by the test circuit, which is implemented off-line. This means that in order to accomplish the test sequence, transmission must be interrupted. An on-line test could also be implemented, with a consequent increment of the circuit complexity. The circuit has an input control pin that allows it to be putted into a stand-by mode, with an almost null power consumption.