EVALUATION OF TEST STRATEGIES IN VHDL DESCRIPTIONS: A CASE STUDY

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1. INTRODUCTION

Current design processes are based on top down methodologies, using hardware description languages as the input of the design flow. This trend motivates changes in the test generation and fault simulation processes in order to establish an efficient method to evaluate test strategies at high abstraction levels. To make this possible it is necessary to adopt a fault model compatible with the circuit or system description.

Several fault models at behavioral or Register Transfer (RT) level have been reported by many authors in the recent last past years. These models are used to estimate, at high abstraction levels, the structural fault coverage obtainable with a specific test strategy.

A fault model at RT level is proposed in [1], for VHDL (VHSIC Hardware Description Language) descriptions. This fault model is based on single and permanent faults, divided in three classes: faults on data, on expressions and faults on statements.

The development of a fault model and a fault injection algorithm are both described in [2], considering that a RT level fault list is a representative sample of the corresponding collapsed gate-level list.

Taken from software testing, a fault model named single bit stuck-at fault is presented in [3]. The authors propose a single-bit stuck-at in an assignment operation at RT level and assume single fault injection with permanent effects. The correlation at gate level is obtained experimentally.

However, there is no a clear relationship between structural faults and RT or behavioral faults.

In this work, we present preliminary results obtained from the evaluation at RT Level of a previously reported test strategy [4]. Both a RTL fault model and a fault injection procedure are adopted in order to obtain the RT level fault coverage that can be later compared with a structural-fault one.

2. TEST STRATEGY

2.1 Circuit under test

The circuit under test (CUT) is a timing circuit composed by cascaded synchronous BCD counters (Fig. 1). Both the CUT and the test circuitry are described in VHDL. In Fig. 2 is showed the interface and entity declaration of the CUT, in Table 1 its state table and finally in Fig. 3 its architecture.

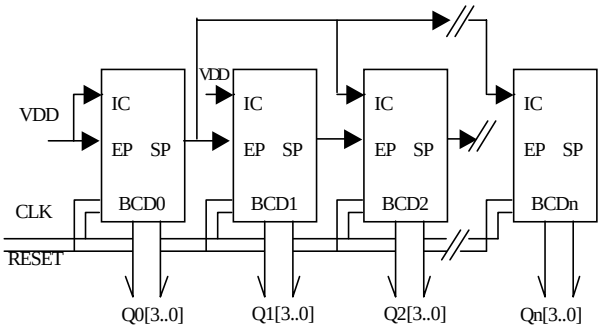
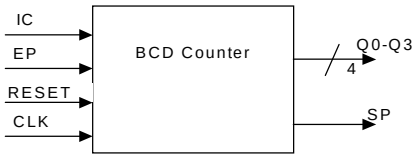


Figure 1. Circuit under test.




```
entity contador1 is
Port (  ic,ep,clk : in std_logic;
        sp : out std_logic;
        q : out std_logic_vector(3 downto 0));
end contador1;
```

Figure 2. Interface and entity declaration of CUT.

EP/ IC / Actual state	00	01	10	11
0	0/0	0/0	0/0	1/1
1	1/0	1/0	1/0	2/0
2	2/0	2/0	2/0	3/0
3	3/0	3/0	3/0	4/0
4	4/0	4/0	4/0	5/0
5	5/0	5/0	5/0	6/0
6	6/0	6/0	6/0	7/0
7	7/0	7/0	7/0	8/0
8	8/0	8/0	8/0	9/0
9	9/0	9/0	9/0	0/1
Next state /output				

Table 1. State table of the BCD counter

```
architecture Behavioral of contador1 is
signal cuenta: std_logic_vector (3 downto 0);
begin
    process(clk, reset, ic, ep)
    begin
          if reset='1' then
          cuenta <="0000";
          elsif (ic='1' and ep='1') then
                if rising_edge(clk) then
                      if cuenta /= "1001" then
                            cuenta <=cuenta+1;
                      else
                            cuenta <="0000";
                      end if;
                end if;
          end if;
    end process;
    process (cuenta, ep)
    begin

          if (cuenta="1001" and ep='1') then
                sp <='1';
          else
                sp <='0';
          end if;
    end process;
    q <=cuenta;
end Behavioral;
```

Figure 3. Architecture of CUT

2.2 Test-mode connection

In test mode, the CUT is divided into its functional blocks (BCD counters) to perform the test. A Multiple Input Shift Register (MISR) is sequentially connected to each functional block by mean of a tri-state bus control system (Fig. 4). Extra circuitry (multiplexers) disconnects the cascade connection and controls the BCD counters. This allows the functional testing of each counter in the system. The CUT's responses are compressed by a MISR into an 8-bits signature. A fault in the CUT is detected if there is a difference between the signature obtained at the end of the test sequence and the signature of the fault-free circuit.

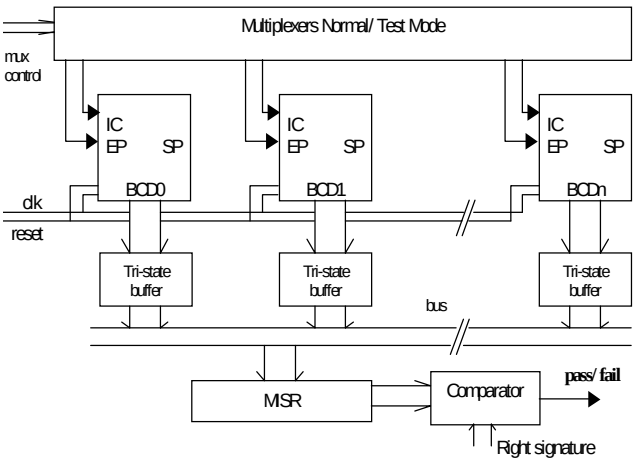


Figure 4. Test mode connection

3. FAULT MODEL

The fault model adopted [3], propose a single-bit stuck-at in an assignment operation at RT level and assumes single fault injection with permanent effects. For signal or variables bit_vector, is injected a logical zero or one in every single element that compounds the vector. Faults in input ports are also considered. Finally, stuck-at faults on the same signal but on different statements are taken to account in different experiments.

To perform the fault injection procedures, two different test sequences previously defined in [4] are adopted (Table 2), and the above-described faults are injected in the VHDL source of the CUT.

Option Number	Exercised sequence		CUT behavior	Verified functionality
	EP	IC		
1	1	1	Count	Count only.
2	1	1	Count	Only two state table conditions.
	1	0	Not enable	

Table 2. Test schedule

4. EXPERIMENTAL RESULTS

The fault injection process is accomplished using standard VHDL features and is carried out using Modelsim, injecting 40 *single stuck-at bit* faults in the source code.

The fault coverage is 75% and 80% for the test sequences proposed. These results are very pessimistic, because our experiments at structural level using a stuck-at

fault model have given fault coverage of 95% and 100% for the same test sequences.

However, it could be considered that some RT level faults lose their relation with gate-level faults during the synthesis and consequently they could be eliminated from the fault list, as is pointed out by the authors in [5]. Nevertheless, this heuristic is not considered here.

5. CONCLUSIONS

In this work has been presented the evaluation of a test strategy in a VHDL description. A RT level fault model has been adopted, and a fault injection procedure has been carried out.

The fault simulation results shown that there is a significant difference between the fault coverage at RT level and the structural –level one. These results could be improved if some heuristics is adopted.

It should be pointed out that the aim of this work is to enhance the knowledge about the behavior of the fault model adopted to predict structural level fault coverage and the results presented are only valid for the proposed case study.

10. REFERENCES

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