A DESIGN-SPACE GENERATION TOOL FOR ANALOG BLOCKS OF ULTRA LOW-POWER IC'S BASED UPON THE BSIM3V3 MODEL

Heiner Grover Alarcón Cubas, Héctor Luis Villacorta Minaya

Microelectronics Group – Pontificia Universidad Católica del Perú

a20020348@pucp.edu.pe, a20020326@pucp.edu.pe

ABSTRACT

The main objective of this work is to present a design tool for the analog basic buildings blocks which, starting from values obtained from SPECTRE output file(working with BSIM3 model) generate a design space for the respective block. The extracted values are stored in tables (matrices, multidimensional arrays) and according to the design specifications established by the designer (minimum gain, FT, L), the tool presented calculates the physical dimensions for the transistors of the analog block (taking into account the parasitic output capacitance) and generates curves required in order to achieve the desired gain and the total power consumption for a given cut - off frequency (FT).

1. INTRODUCTION

In recent years, many different design methodologies for enhancing the traditional analog design of analog CMOS IC have been developed [1][2]. In that trend, several models that describe the operation of the MOS transistor were born: EKV, ACM, BSIM; the latter being the model we used to develop the tool presented.

The motivation for developing this tool responds to the need for improving the methodology of design that has been in use in recent years. Our tool is a method that allows us to minimize the time spent on the design stage and, above all, achieve major accuracy in the results. This is how we decide to come up with a tool such as the one that exists for the model ACM[3], but based on the BSIM3 model and targeting the 0.35u AMS CMOS process. Thus, working with the gm/ID methodology design [4], which provides a simple method to calculating the physical dimensions of the transistor, we elaborated a group of routines that will permit the extraction of the necessary parameters from the SPECTRE output file, in order to obtain the desired curves to generate the design space for the required transistor/analog block.

This document is presented as follows: in section 2 we explain the procedure for the extraction of design parameters and the generation of the design space curves [2]. In section 3, we introduce the design of a symmetric OTA and a common source amplifier. In section 4 we present the results of the two designs mentioned before. Finally in section 5, we make some conclusions we have been able to establish.

2. PROPOSED METHODOLOGY

2.1.- Parameters Extraction and outline of the gm/ID vs. ID(W/L) curve

The first step into the elaboration of this tool is to carry out the necessary simulations of the MOS transistor (characteristic curves), in order to utterly work with the results obtained, based upon the SPECTRE output file. Then the extraction of key parameters (Vgs, Ids, L, Vds) is performed by means of routines that handle files inside the MATLAB environment. These values are stored in matrices and/or multidimensional arrays that are useful to perform the necessary operations in order to obtain the most important curves of the gm/ID methodology with the aid of the features provided by MATLAB. The gm/ID vs. ID/(W/L) curve for a N type MOS transistor is shown in figure 2 and as it is well known, we can determine the transistor inversion level coefficient and its physical dimensions. Likewise, it is possible to calculate de Early voltage (VA)[5], by tracing the VA vs. gm/ID curve.

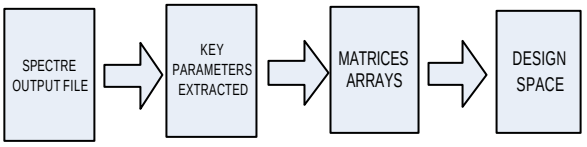

Figure 1: Tool flow; extraction of parameters from the text - files.out until the generation of the design space

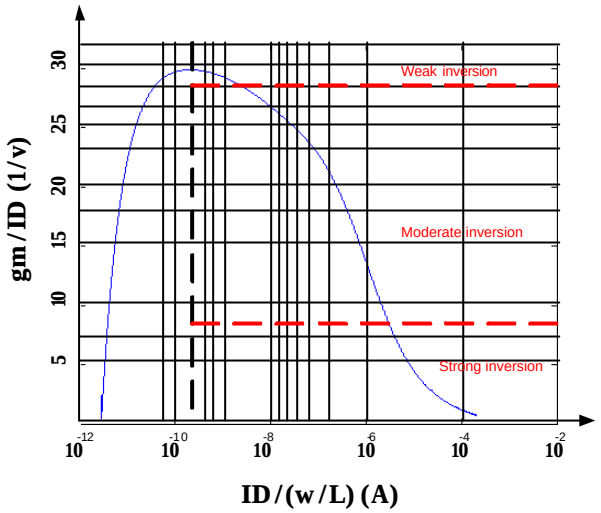

Figure 2.- gm/ID vs. ID//W/L) curve
Transistor NMOS

2.2.- Design space

Now, what we look for is to explore the design space of the analog block and in order to do so, we have to work with the Av vs. gm/ID, Av vs. L, ID vs. gm/ID, W vs. ID, C vs. gm/ID curves[2], and lying upon the design specifications entered by the designer, such as: gm/Id, L, Av min, FT.

Since we already have the gm/ID and VA values stored up in bi-dimensional matrixes to different values of L, we can sketch for the Av vs. gm/ID curve, as follows:

$$Av = \frac{gm}{ID} * VA \quad \ldots\ldots\ldots (1)$$

According to the input parameters, i.e: a predetermined gm/ID and desired L, we can establish the respective gain for this block, as seen in figure 3.

Now, to generate the Av vs. L curve we must indicate that according to (1) the obtained gain is independent of frequency, since we have gm/ID as an input parameter.

The ID vs. gm/ID, W vs ID, C vs. gm/ID curves are sketched for different frequencies, which can be entered by the user. An algorithm was set for generating intermediate frequencies with a 1-decade interval, whenever a maximum and minimum frequency are entered.

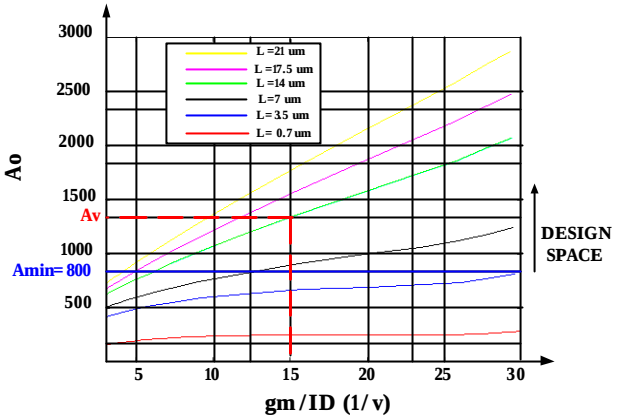

Figura3.- Curva Ao vs. gm/ID
Transistor NMOS

In the curve, we show the optimal current consumption for various frequencies and we can determine the level of inversion as well.

For this curve, we used the gm/ID and ID/(W/L) matrices and arrays taking into the parasitic capacitance[2] regarding the output of the analog block that has to be designed. For this, we made use of an iteration-based algorithm[2] where the gm and ID values are constantly modified to fit the different frequencies, and the different values of W are calculated for a given value of L, and setting a fixed a load capacitive according to the needs the designer.

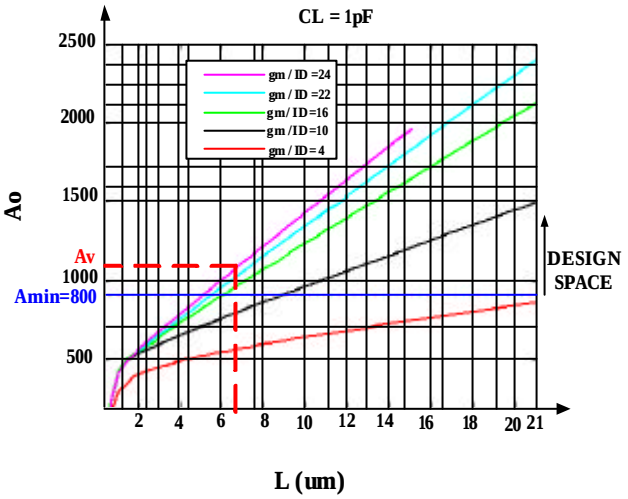

Figure 4.- Ao vs. L, NMOS Transistor
CL=1pF,Avmin=800

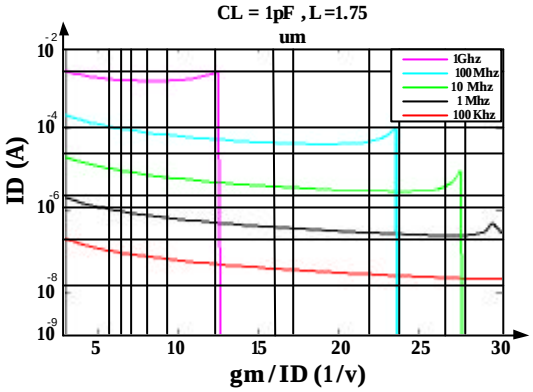

Figure5.- ID vs. gm/ID, NMOS Transistor
Vertical lines indicate no solution for other gm/ID values

The last two curves are of special interest to appreciate the great impact of parasitic capacitance at high frequencies (gm rises), and the subsequent increase on the value of W for any given value for L.[2]The curves are generated based on parasitic capacitance calculation (Cp), where an loop iterative for any given L and gm/ID and through different mathematical operations sweep the values of gm and Id for different frequencies, and with the aid of interpolation of the gm/ID and ID/(W/L) matrices and arrays, we obtain the values of W and C (C=CL + Cp) for any given fre quency.

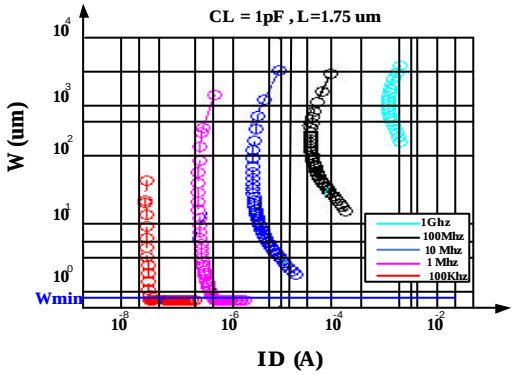

Figura6.- W vs. ID

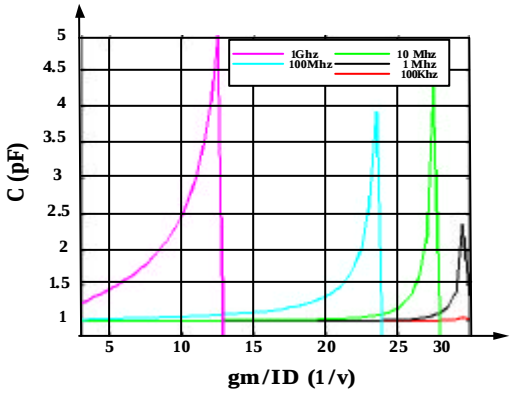

Figura7.- C vs. gm/ID

3.EXAMPLE OF DESIGN

3.1. Design of a Symmetric OTA

In order to prove the validity of our tool, we shall analyze the architecture of a symmetric OTA [2][6][7], which was selected beforehand to for implementing a pass-band filter of a sensing channel from a pacemaker. The circuit is shown in figure 8.

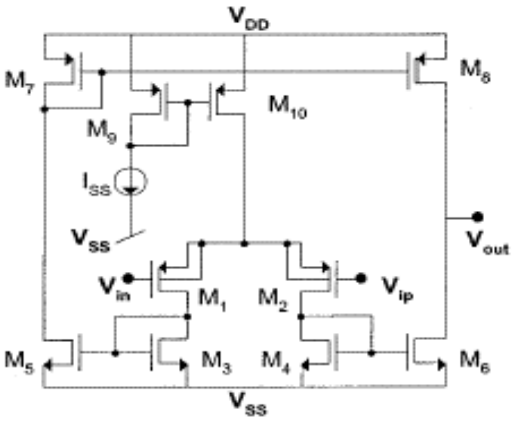

Fig. 8: Architecture of a symmetric OTA

The steps made in the design of a symmetric OTA, using the gm/Id methodology, are shown in the following.

First, the value of the overall OTA transconductance is determined: Since Gm=gm1=gm2, where gm1 and gm2 are the transconductances of M1 and M2 respectively, we will design those transistors in the first place. We will pick a gm/ID value on the gm/ID curve taking into account the level of inversion on which the transistor shall operate. We will design the OTA to operate inside the moderate inversion zone, setting a gm/ID value of 20. Moreover, since we are currently working with the topoly shown in figure 8, we must never leave aside the fact that M1 and M2 are P-type transistors.
The bias current is obtained as follows:

$$ID = \frac{Gm}{gm / ID} \quad ...(2)$$

Where the current to which M1 and M2 are biased is half the current of the Iss source. Our tool receives as input parameters the transistor type and its inversion level, information that is used to calculate the value of the normalized drain current. Finally, based on the calculated parameters we proceed to find aspect radio.

3.2. Design of A Common Source Amplifier

In order to design the amplifier we assume the following specifications: the DC gain (Av), transition frequency (fT) and a value for L is determined. After entering these parameters we obtain a value for Gm/Id, which will be useful to calculate the drain current on the circuit as well as the value for W.

4. EXPERIMENTAL RESULTS

In the case of the common source amplifier, we sweep around the whole design space as shown in figure [2], in order to test the validity of the methodology using SPICE. In table 1, the values obtained are shown for Gm/ID=10 and L=1,75 µm.

Table 1

fT(Hz)	Id(uA)	W(um)	Av	FTspice(Hz)
100k	0,1	1	470	100k
1M	0,7	7	470	1M
10M	5	50	470	10M
100M	80	800	470	100M

In the case of OTA, the values obtained for L=1,15 um are shown in table 2.

Table 2

Transistor	Id(uA)	VA(V)	W/L	Gm(us)	Gds(us)
M1,M2	25	37,13	57,389	325	0,673
M3,M4,M5,M6	25	56,44	7,375	200	0,4429
M7,M8	25	37,19	10,857	150	0,6668
M9,M10	50	37,19	21,716	300	1,3336

$$Av = (gm / Id) * (VA_6 // VA_8) ...(3)$$

For these values, we obtained of equation 3 a gain Av=291,23, value that is later compared with the that obtained from the SPECTRE simulating BSIM3V3, which resulted in a gain of 270, and thus an error of 7.86%. This procedure fully valides the good performance of our program.
In the table 3 are shown the results for a GM =16,336nS

Table 3

Transistor	Id(nA)	W(um)	L(um)
M1,M2	0,817	0,8	78,4
M3,M4,M5,M6	0,817	0,8	78,4
M7,M8	2,63	0,8	39,2
M9,M10	0,817	0,8	78,4

5. CONCLUSIONS

Regarding the common source amplifier, it is evident that not only did the simulations on the SPECTRE agreeded on the fT, but they also agreeded on the Dc gain which provides on great reliability on the usage of this tool.
Regarding the OTA, the results are also satisfactory, given the differences between the analytical results and the simulation results.

6. REFERENCES

[1] Daniel Foty, David Binkley, and Mathias Bucher, "Starting Over: gm/Id-Based MOSFET Modeling as a Basis for Modernized Analog Design Methodologies", ECCTD'01 August 28 - 31, 2001 Espoo, Finland.

[2] Fernando Silveira, Alfredo Arnaud, Conrado Rossi, "Diseño de Circuitos Integrados para dispositivos médicos implantables", CVIT, 2004. http://oaid.uab.es/cvit

[3] Carlos Galuo Montoro, M.C Schneider, Cátia dos Reis Machado, "Analog Design Tool based on the ACM model"

[4] F. Silveira, D. Flandre, P. G. A. Jespers, "A gm/ID Based Methodology for the Design of CMOS Analog Circuits and Its Application to the Síntesis of a Silicon-on-Insulator Micropower OTA", IEEE Journal of Solid State Circuits, Vol. 31, No. 9, September 1996.

[5] Fernando Paixão Cortes, Eric Fabris, Juan Pablo Martinez Brito, Sergio Bampi, "Análise e Projecto de Módulos Amplificadores e Comparadores em Tecnología CMOS 0.35µm", IX Workshop Iberchip, La Habana, Cuba, 26 al 28 de marzo de 2003.

[6] A.Veeravalli, E.Sánchez-Sinencio, J.Silva-Martínez, "Transconductance Amplifiers Structures With Very Small Transconductances: A Comparative Design Approach", Ieee Jssc, Vol.37, Nº.6, Jun.2002.

[7] S. P. Jiménez, Et Al. "Design Of Operational Transconductance Amplifiers With Improved By Using Graded-Channel Soi Nmosfets".