LOW VOLTAGE, LOW POWER, SELF-CLOCKED SINGLE-POLY CMOS COMPATIBLE OTP MEMORY SYSTEM

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ABSTRACT:

A single poly non-volatile memory system for low voltage, low power analog calibration applications is presented, which performs the read, program and verify operations for a single-poly non-volatile memory. The reading circuitry performs single-ended sensing, thus no dummy cells are required. Furthermore, the system addresses the cells sequentially and automatically, is self-clocked and the operation frequency is adjustable. The system was fabricated using 0.35µm technology (nominal voltage of 3.3V). It operates down to 0.95V with a power consumption of 600nW during the reading operation. The timing unit operates down to 0.55V.

1. INTRODUCTION

A memory system for a low voltage, low power analog calibration application is presented. The system performs the read, program and verify operations for a single-poly non-volatile memory. The features of the designed system include: low voltage, low power operation, automatic self-clocked sequential memory access with adjustable operation frequency by means of CMOS delay elements, program-verify control, non-volatile data storage by means of single-poly CMOS-compatible memory cells, and single ended sensing. The system was integrated using 350nm technology (nominal operation voltage=3.3V).

The system is intended to be used for the analog calibration of a smart label, thus the system must be fabricated at low cost. The single poly non-volatile memory can be very easily integrated at low cost using standard CMOS fabrication processes and thus is appropriate for many embedded applications.

In the following paragraphs, the system and the features mentioned above will be described, and other possible applications will be discussed. Measurement results are also provided.

2. DESCRIPTION OF THE SYSTEM

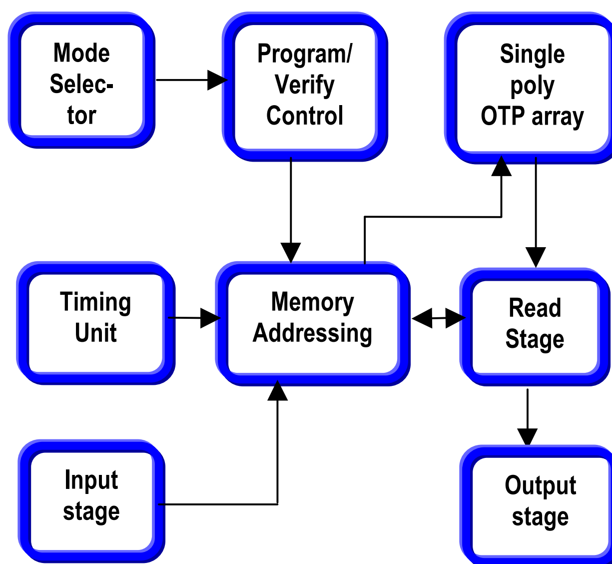

Figure 1. Block diagram of the designed system

2.1 Basic Operation

Figure 1 presents a simplified block diagram of the designed system. The mode selector sets the system to the program or read mode. Since the system will be embedded into a smart label, it is necessary to perform the reading operation at low voltage, low power operation conditions, and that the reading is performed as automatically as possible. Due to the high frequency operation of the RF front of the label, it is not advisable to derive the clock signals from the RF front, since the power consumption of the frequency division blocks would be too high for the application. Besides, the system must operate at very low frequencies since the RF front requires some time to reach a steady stage after each calibration step (minimum clock cycle: 64µs). For this reason, the design includes a timing

unit which is responsible for the generation of all clock and control signals for the read and the program/verify operations, independently of the operation frequency of the RF front.

The timing unit controls the memory addressing unit, which performs automatic, sequential addressing of the memory cells in the memory array. For the read mode, cells are simply addressed and the sense amplifier senses the cell contents at a frequency determined by a control voltage of the timing unit. Once all cells have been read, the circuit automatically stops its operation and the stored data is available at the output registers included in the reading circuitry block.

During the program/verify operation, cell addressing depends on the output of the sense amplifier and on the contents of the input registers.

2.2 Single Poly CMOS Compatible OTP Memory Cell

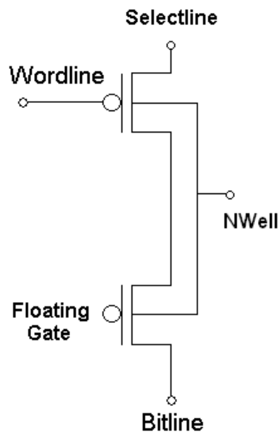

Figure 2. Schematics of the single-poly OTP memory cell

CMOS compatible non-volatile memory cells can provide a cheap alternative to integrate memories in system on chip and ASIC applications. The requirement of double poly gates and other modifications of conventional transistors in order to enhance the physical mechanisms responsible for the programming and erasing operations, lead to the modification of standard CMOS base processes by including additional masks and fabrication steps. With this, the cost of integrating non-volatile memories significantly increases the cost of mask production and circuit integration, and makes more difficult to integrate embedded non-volatile memories. In this system, an OTP memory cell based only on standard PMOS transistors [1,2] is used. Hence, no new library elements need to be developed, and no new structures, masks or process steps must be added to the process.

The cell's schematic is presented in figure 2. The cell characteristics before and after programming are shown in

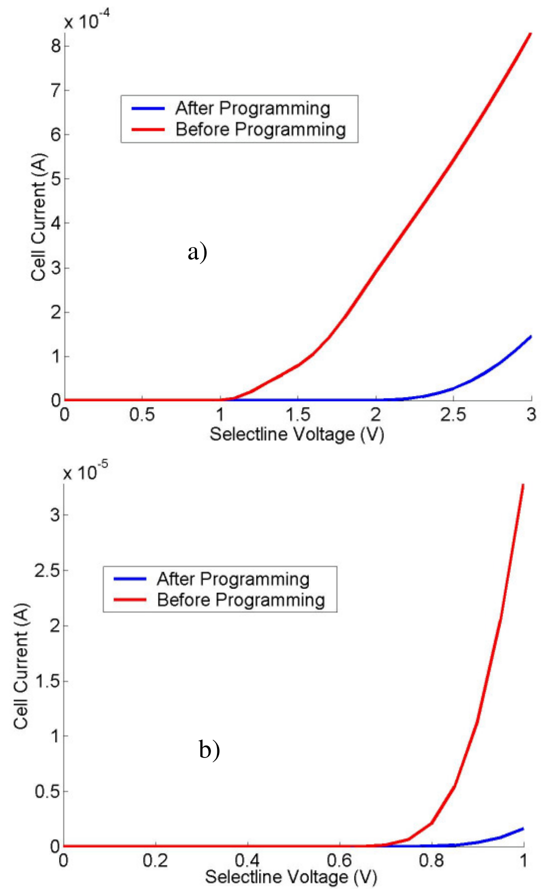

Figure 3. Measured cell characteristics before and after programming for operation at a) 3V, b) 1V.

figure 3 for operation at 3V and 1V. The measurement conditions for the cell's characteristics were Vselectline= 0..3V, Vnwell= 3V, Vwordline= 0V, Vbitline= 0V for graphic 4a) and Vselectline= 0..1V, Vnwell= 1V, Vwordline= 0V, Vbitline= 0V for figure 4b). Figure 4b) shows a clear difference in the cell current for a programmed and an unprogrammed cell for operation at 1V. The cell is programmed by means of drain avalanche hot electron injection and can be programmed at Vselectline= 4.5V, Vwordline= 1.5V, Vnwell= 4.5V and Vbitline= 0. The programming time is 15ms.

An additional advantage of the cell is the relatively low programming voltages (maximum 4.5V) as compared to its NMOS counterpart (with a programming voltage of 6.5V) and other single-poly approaches.

As an example of the economical advantage of integrating this memory using a standard CMOS process, the integration cost per square milimiter of a memory syystem using the standard CMOS process can be reduced in 28% [3a, 3b] compared to the cost using an EEPROM process with the same feature size and from the same manufacturer. In some cases, the cost can be reduced up to 65% [3c].

2.3 Self-clocked automatic sequential memory access with adjustable operation frequency

Self-clocked operation is achieved by means of the timing unit, which generates and synchronizes basic control signals and determines the operation frequency of the system.

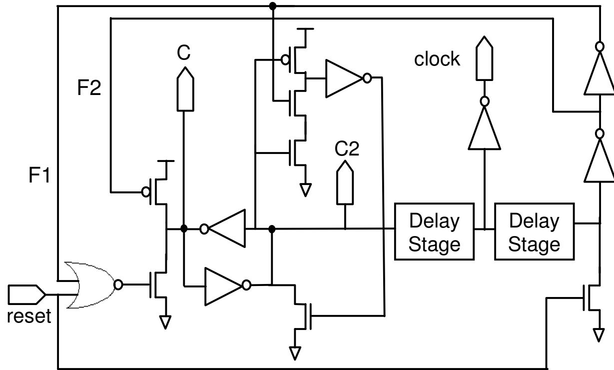

Figure 4. Simplified schematic of the timing unit

Figure 4 presents the schematics of the timing unit. It basically consists on a feedback system controlling an SR latch. Operation of the timing unit starts with a reset pulse (active high), and continues until all cells have been addressed. The feedback signals, together with the reset signal, determine the waveforms of the output signals clock, C1 and C2. These three output signals are the basic signals from which all other control signals of the system are generated.

The timing unit operates as follows: reset signal, together with a feedback signal F1activates the first NMOS transistor, which reset a latch made up of two cross-coupled inverters. C1 is later used to control the operation of the sense amplifier in the reading stage. C2 and F2 controls activate an NMOS transistor to set the latch. C2 is also fed to the first delay stage, and the first stage controls the second delay stage. The inverters that generate F1 and F2 from the output of the delay stage fulfill both logic and signal-restoring functions since the output level for a "1" signal at the delay stages is determined by the control voltage applied to the delay stage.

Figure 5 presents the circuit schematic of the delay stage, which is based solely on MOS transistors, thus providing a compact, low power delay element. When the input signal is low, M1 and M3 are active, and thus M5 is off and M6 is on. Since the inverter conformed by M3 and M4 is powered by Vcontrol, the time that transistor M6 will require to discharge the output node can be controlled with help of Vcontrol. When the input signal is high, M2 and M4 are active, hence M5 is on and M6 is off. M5 will charge the output node up to the level of the control voltage. The time required to charge the node is again controlled by Vcontrol. The complementary transistors M5

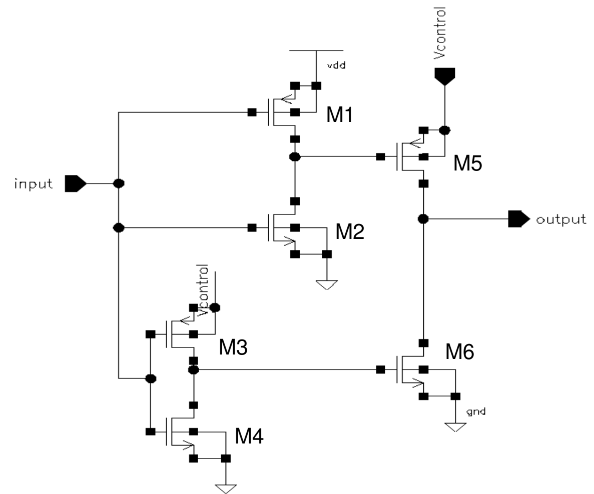

Figure 5. Schematics of the delay stage. Transistor dimensions: M1, M3, M4, M5 M6=0.6μm/0.35μm; M2=0.6μm/0.6μm

and M6 may operate down to the subthreshold region according to the magnitude of the control voltage. The time required to charge the output nodes allows controlling the operation frequency.

The timing unit feeds a counter whose outputs are decoded with help of some additional logic to address the cells in such a way that they are active only the necessary time required by the sense amplifier and the output stage's registers to latch the cell's contents, providing a stable signal at the output stage. This reduced activation time avoids unnecessary power consumption during the reading operation.

2.4 Program-verify operation

Due to the low operation voltage during the reading operation (Vdd $\leq$ 1V), it is necessary to ensure that the programmed cells can be distinguished from the unprogrammed cells during the reading operation. Thus, a certain current level must be achieved such that the sense amplifier can distinguish programmed from unprogrammed cells. For this reason, a program-verify operation is necessary.

Cells are programmed only when its corresponding input data at the input stage is "0". During the sequential access, the programming bias will be applied to the corresponding cell. Level shifters adjust the wordline voltages of the other cells to deactivate them. The memory array is isolated from the sense amplifier during the programming operation. The programming time is fixed by the operation frequency of the system.

After the first programming cycle, the cell is read at the bias conditions of the reading operation. If the cell's current is still not high enough, the programming operation is repeated again. This program-verify cycle is repeated

until the cell reaches the required current level. During the verify operation, the output of the sense amplifier is fed to the addressing stage to keep the current cell addressed or to address the next cell, according to the output level of the sense amplifier.

Cells which do not require to be programmed, that means, its corresponding input data at the input stage is "1", are simply skipped from the addressing sequence.

Another important function of the program-verify operation is related to the data retention of the cells. Since the cells are programmed using hot carrier injection, they suffer more degradation than conventional memory cells based on Fowler-Nordheim tunneling operation. The program-verify operation also contributes to ensure that the cells are not programmed more time than the necessary, and thus limits the damage caused by hot carrier injection. This contributes to improve the data retention, since the oxide is in better conditions to retain the injected carriers.

2.5 Single-ended sensing

The sense amplifier is shown in figure 6. The circuit is single-ended and since it does not perform differential sensing, it does not require a dummy cell.

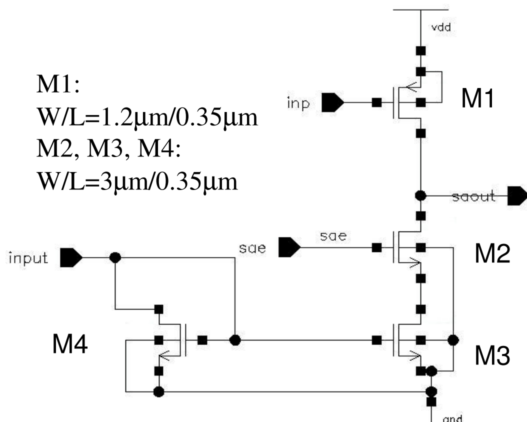

Figure 6. Sense amplifier for single-ended sensing.

Transistor M1 is activated by the signal INP and precharges the output node to the "1" level. Transistor M4 is the input transistor of the sense amplifier and is connected to the memory array during the reading operation, thus providing the cell's current a path to ground. M4 and M3 form a current mirror. Transistor M2 is enabled by the signal SAE and provides a current path between Vdd and gnd at the output of the sense amplifier. During the sensing operation, both M1 and M2 are active. If the addressed cell is programmed, its threshold voltage should be low enough to have a cell current such that at low supply voltage the mirrored current through M3 can discharge the output node. If the cell is unprogrammed then the cell's current is low, and the current through M3 is not enough to discharge the output node, which will be kept at Vdd as precharged by transistor M1.

3. MEASUREMENT RESULTS

The timing unit operates down to a supply voltage of 0.55V and the minimum control voltage is 0.3V. Figure 7 shows the output of one of the control signals for the reading/program-verify operation under this minimum voltage condition.

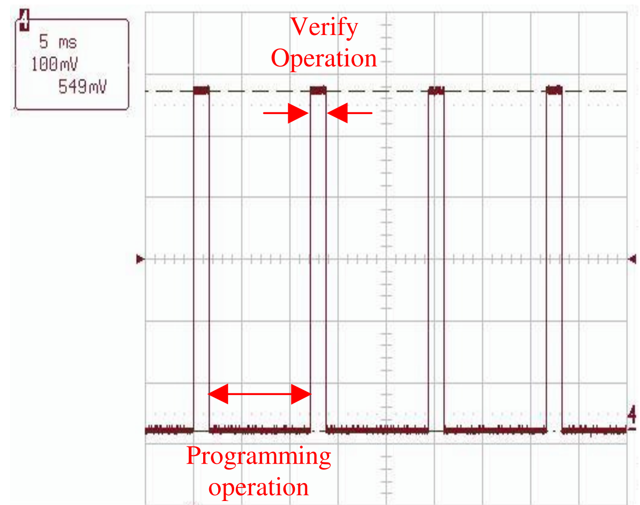

Figure 7. Oscillogram of operation at 0.55V. The signal shows the programming and read/verify intervals

During the reading operation, the circuit will be active when the signal is high. During the rest of the time the system will wait for the next positive edge to access the next cell. This provides time for the RF system to stabilize after the applied calibration step.

During the program-verify operation, the cells will be programmed when the control signal is low, and read for verification when the control signal is high.

The power consumption during the reading operation at different supply voltages is summarized in Figure 8. The minimum supply voltage for operation of the whole circuit is 0.95V. At this supply voltage, the circuit consumes 600nW, and the operation period is 604µs. With this, the timing unit operates at a lower voltage than [4] and the whole circuit operates at much lower power than [4]. The operation frequency of the system can be varied in a large range by adjusting the control voltage between a minimum of 0.3V and a maximum of Vdd. As an example of the range of adjustable frequency, figure 9 hows the operation frequency vs control voltage at a supply voltage of 0.75V.

The complete memory system occupies an area of 225x345 μm^2. Figure 10 presents a microphotography of the chip containing the system.

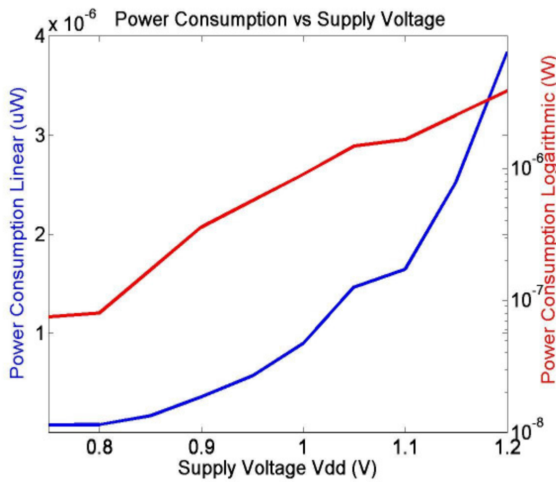

Figure 8. Measured power Consumption vs supply voltage

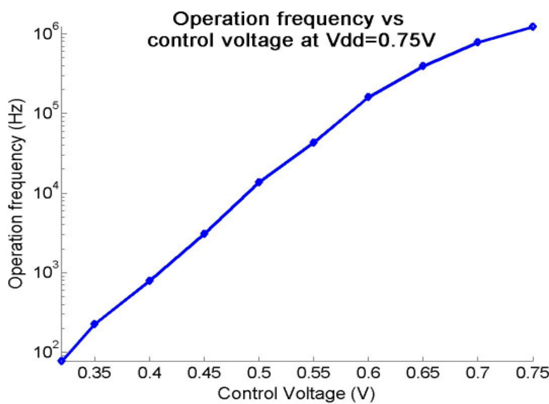

Figure 9. Measured operation frequency vs control voltage at Vdd=0.75V

4. CONCLUSIONS

The system was designed according to the requirements of analog calibration of an RF front. The OTP memory array stores the calibration data for the sequential activation of the different sectors of the calibration circuitry, which would perform the impedance compensation of the RF front. Such compensation may improve the power transfer to the smart label and thus increase the minimum detection distance of the smart label or smart card. In addition to the low voltage and low power requirements of the application, other constrains for the design were the cost and the compatibility with CMOS processes, which are also fulfilled by means of the single-poly CMOS-compatible non-volatile memory cells. For this application, OTP memory cells were required, although the memory system

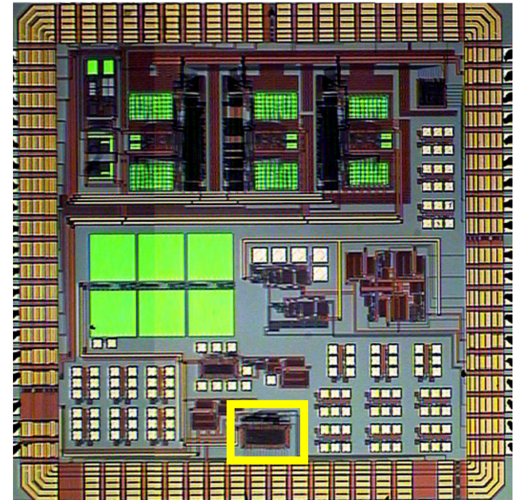

Figure 10. Microphotography of the chip TUHCR, which contains the designed system, shown by the yellow rectangle

can also be implemented using EEPROM non-volatile memory cells. However, in this case the cells would require supply voltages higher than 1.5V. For details about operation and optimization of these cells, the reader is referred to [2,5].

Other possible applications of the proposed system include configurable commercial subproducts, identification memories for wafer traceability, smart cards and labels, and especially analog calibration, due to the sequential access of the memory contents. The circuit consumes low power and can be operated at low voltage, is easy to use, and can be easily and cost-effective integrated into embedded circuits, due to the full CMOS compatibility of the memory cells.

5. REFERENCES

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