Electrical Analysis and Modeling of Resistive Opens in CMOS Technology

M. Renovell[1], M. Comte[1], Ilia Polian[2], P. Engelke[2], B. Becker[2]

1. LIRMM-UMR C5506 CNRS
161, rue Ada
34392 Montpellier Cedex 5 France

2. Albert-Ludwigs University
Georges-Köhler Allee 51
79110 Freiburg im Breisgau, Germany

Abstract

In modern deep submicron process, resistive open belong to the category of frequent defects and exhibit a complex behaviour. This paper analyzes the electrical behaviour of this type of defect as a function of its unpredictable resistance. It is demonstrated that the electrical behaviour depends on the value of the open resistance. It is also shown that detection of the open by a given vector Ti in a sequence depends on all the vectors that have been applied to the circuit before T1 making the detection a quasi-infinite sequential problem.

1. Introduction

The advent of integrated circuit technology has introduced electronics in many aspect of present-day life. As the use of electronic components increases, the expectation of lower cost, better accuracy, and higher reliability increases. Lower cost and better accuracy is achieved by putting more transistors per unit of silicon, using design automation, increasing device operation speed, and reducing its power consumption. However, these design steps cannot guarantee reliability. In fact, as the circuit density increases, the probability of a manufacturing defect increases. The higher expectation of reliability can only be met by more thorough and comprehensive testing.

Due to the complexity of IC technological process, many physical defects occur during the manufacturing of any system. The typical defects encountered in today technologies and modeled in yield simulators are the so-called spot defects that may cause shorts and/or opens at one or more of the different conductive levels of the devices. Test generation for any type of defect is obviously not feasible due to the huge amount of CPU time and memory size required. Instead, test generation relies on fault models that are supposed to both represent the defect behavior and allow easy generation of test vectors through ATPG and fault simulation.

Classical fault models (stuck-at, stuck-open, stuck-on …) have been proved to be efficient for the analysis of many of these faults. However, it is well-known that these fault models cover only partially the spectrum of real failures in today's integrated circuits. The increasing demand of low ppm defect rates requires the derivation of ever more accurate fault models. In particular, a special attention must be paid to defects that exhibit complex behavior not accurately represented by classical fault models and defects with a high probability of occurrence. In modern nanometer processes, resistive opens belong to both categories since (i) they change some of the electrical features of the connection, and (ii) they are predominant defects in today technologies in which copper is used for interconnections.

A number of research works have been conducted in the past years dealing with the electrical characterization and modeling [1-9] of this kind of failure. Classically, it is considered that the connection is fully open, i.e. the following gates are completely disconnected and called 'floating gates'. In this paper, we analyze the case where the following gates are still connected but through a degraded line exhibiting some resistance. It is important to note that the resistance of the open is an unpredictable parameter of the defect. The electrical behavior of the defect obviously depends on this random parameter as well as its detection conditions. In order to optimize and guarantee the detection of such defect, its electrical behavior has to be analyzed as a function of this random parameter and optimal detection conditions must be derived.

The paper will be organized as follows. Section 2, gives some general definitions on detection of defects exhibiting random parameters, the resistive open being a particular case of this class of defect. In section 3, the electrical behavior of the resistive open is analyzed considering a sequence of 2 test vectors, then considering a sequence of n test vectors. Finally, Section 4 gives some concluding remarks.

2. Defects with random parameters

In today technologies, many metal layers allow to implement connections between logic gates. This high

connection density makes the defects affecting interconnect predominant. These opens may be of two classes:

- the fully disconnected open leading to floating gate transistors,
- the partially disconnected opens leading to resistive open connections between logic gates.

In the past, fully disconnected opens have been extensively devised in the literature [2,3,5,8]. Due to different process problems such as incomplete oxide etching mainly when copper is used, many resistive opens are today encountered in the manufactured chips and so, there is a need for a specific study of this defect.

Figure 1 gives an example of an extremely simple circuit where logical node n4 is affected by a resistive open. This didactic circuit has 4 inputs (I1,I2,I3,I4) and 2 outputs (O1, O2). Note that we do not care for the logic function implemented by this circuit, we just need a simple example to conduct our electrical analysis. Obviously, the demonstrations given here may be extended to real cases.

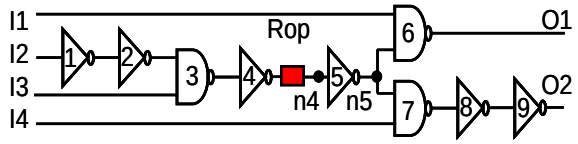


Figure 1: A resistive open

It is well known that partially disconnected opens exhibiting intermediate resistance values can not be detected by a static Boolean testing strategy because the logic nodes always end with their correct logic value (Vdd or Gnd) implicitly assuming a slow frequency test. But in turn, they affect the timing behavior of the chip and so they can be detected by a delay testing strategy.

Considering delay testing, i.e. dynamic voltage testing, Figure 2 gives the SPICE simulation of the dynamic behavior of the defect free circuit of figure 1. Simulations are performed in a 180nm technology. In this simulation T0=1011 and T1= 1111, i.e. only input I2 switches from 0 to Vdd at time t0=0.

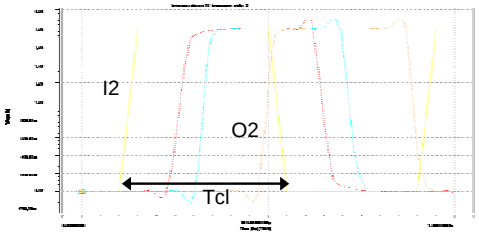


Figure 2: Defect free dynamic behavior

The circuit operating frequency is determined by the critical path composed in this example of gates: 1,2,3,4,5,7,8, 9. In the example of figure 2, the critical path is activated and ouput O2 switches from 0 to Vdd. It appears that the circuit may operates at Tcl=0.4ns with a small but reasonable security margin.

We perform now another simulation with two different vectors: T0=1010 and T1=1110, illustrated in figure 3. Only input I2 switches from 0 to Vdd but, in this case, the rising edge is propagated to output 01 through gate 6. So, the rising edge of I2 is propagated through the circuit resulting in the following definitions:

- Tpb (Time Propagation Before the defect),
- Tpa (Time Propagation After the defect),
- Tsl (Slack Time of path I1=>O1),
- Tcl (Clock Period for the CUT.

The rising edge of input I2 reaches the defect in a period of time called Tpb=0.135ns, this propagation time before the defect depends on the used propagation path: gates 1-2-3-4 in our case. Then the edge propagates from the defect to output O1 in a period of time called Tpa=0.065ns, this propagation time after the defect depends again on the used propagation path: gates 5-6 in our case. After its rising edge, output O1 stays stable for a period of time equals to Tsl=0.2ns before to be latched, assuming some output register.

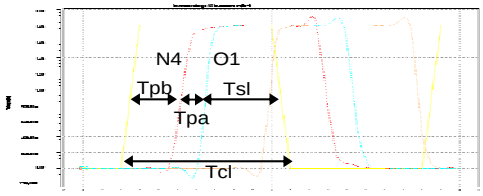
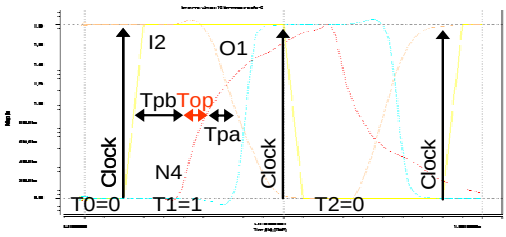
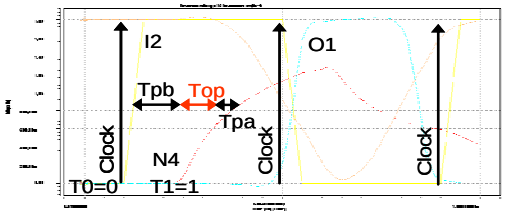


Figure 3: Defect free path to O1



a) Small Resistance Rop=3KΩ



b) High Resistance Rop=9KΩ

Figure 4: Dynamic behavior of a resistive open

As classically stated, a timing defect must have a 'size' (Top) larger than the slack time (Tsl) to be 'detectable'. The size Top of the defect is, in our case, a function of the open resistance value Rop. The resistance is a random parameter of the defect and can not be predicted, but we can simulate different cases of resistance value. Figure 4.a gives an example of open where the value of the resistance is quite small R=3KΩ. It clearly appears that the signal at node N4 is slightly degraded, it is slower than its defect free counterpart, an additional delay Top=0.13ns appears. But the size of the timing defect is still smaller than the slack time, a correct output value on node N5 is latched in the register and the circuit operates correctly. Figure 4.b gives another example where the value of the open resistance is higher R=9KΩ. In the latter case, the size of the timing defect is larger than the slack time and a faulty output value is captured in the output register. The open is detected.

The above simple simulations demonstrate that detection of the open depends on its random resistance. We understand that the objective of a good quality sequence would be to cover as much as possible the complete domain of the random parameter of every considered resistive open.

Consequently, to optimize the quality of a test sequence for resistive open, it is very important to:

1) Analyze the electrical behavior of the open as a function of its unpredictable resistance.
2) Determine the full range of detectable resistance GDI for a given resistive open.

3. Detection conditions for resistive opens

From figure 4, it is clear that an open with a small resistance (3KΩ) is not detected while an open with a large resistance (9KΩ) is detected. This means that a given range of 'large' resistances may be detected. The objective of this section is:

i) to determine the range of detectable resistance,
ii) to identify parameters that influence this range.

3.1. Detection with a pair of vectors

In the previous example, a pair of vectors is applied to the circuit: T0=1010 followed by T1=1110. The smallest detectable resistance by (T0,T1) is a resistance value such that the additional delay Top is equal to the slack time:

$$Top = Tsl = Tcl - Tb - Ta$$

In our example, SPICE simulations show that the smallest resistance is equal to Rop^{min}=7.5KΩ. In other words, any open with a resistance larger than 7.5KΩ can be detected by the pair (T0,T1). An open with a smaller resistance creates an additional delay which is too small to be detected by (T0,T1).

Note that the above range is associated to the pair of vectors (T0,T1). But, another pair of vectors may detect even smaller resistances. This will be the case if another propagation path is excited with a smaller slack time.

3.2. Detection with a sequence of n vectors

Now, we do not consider only 2 vectors but a sequence of several vectors applied to the circuit of figure 1, i.e. several cycles. The sequence is made of 1 initial vector (T0) and a sequence of 6 successive vectors (T0,T1,T2,T3,T4,T5,T6) with T0=0010, T1=0110, T2=0010, T3=0110, T4=0110, T5=0010, T6=1110. It can be observed in the sequence that:

- Input I3 is equal to 1 making propagation through gate 3 always possible in the 6 cycles,
- Input I4 remains at 0 making propagation through gate 7 not possible, and so output 02 remains at 0.
- Input I1 is equal to 0 for 5 cycles (T0 to T5) making propagation through gate 5 not possible during the first 5 cycles. Then input I1 switches to 1 in the sixth cycle making propagation possible.
- Input I2 successively switches from 0 to 1, 0, 0, 1, 1, 0 and 1.

In this simple and didactic example, node N4 is observable on output O1 only during the 6^{th} cycle when I1=1. We can imagine that vector T6 has been generated on purpose, i.e. to detect a fault on node N4 and so making node N4 observable. While the previous vectors (T1,..T5) have been generated targeting some others faults.

During the first 5 cycles, node N4 is not observable but, according to the whole logic activity of the circuit, it may switch from 0 to 1 or from 1 to 0. The successive input vectors may create successive transitions of node N4. In our small example, node N4 just follows input I2 because gate 3 is always transparent.

In the fault-free circuit node N4 switches from Gnd to Vdd and vice-versa, but in the faulty circuit the signal is degraded by the resistive open. Two cases may appear:

- If the resistance of the open is small, the signal is slower but it is still able to reach the power and ground values. The circuit operates as a fault-free circuit.
- If the resistance of the open is large enough, the signal is slower and it may not be able to reach the Vdd/Gnd value before the next transition as illustrated in figure 5 with Rop=7KΩ.

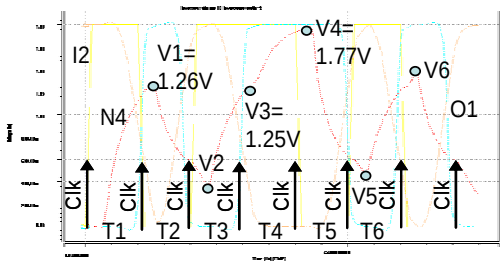


Figure 5: Dynamic behavior through a sequence

Lets explain this case with the example of figure 5. Input I2 is initially equals to 0 (T0) and switches to 1 (T1) at time t0. At time t0+Tbp (propagation time before the defect), the rising transition reaches the output of gate 4 and so node N4 starts switching V(t).

Due to the resistance of the defect, the time requires by V(t) to reach Vdd is much higher than the cycle time Tcl. At time (t0+Tcl), input I2 switches from 1 to 0 (T2) and, this new transition reaches node N4 at time (Tcl+Tbp). This new transition interrupts the previous one even if node N4 is not yet arrived to Vdd. Consequently, we observe that, during the first cycle, node N4 switches from V(t0)=V0=0V to V(t0+Tcl)=V1=1.26V.

Obviously, we can make the same demonstration for the second cycle at time (2Tcl+Tpb), the third at time (3Tcl+Tpb)… We globally observe in figure 6 that node N4 is going from V0, to V1, to V2… to V5. At time (t0+5Tcl), when vector T6 is applied to detect the resistive open on node N4 (remember that node N4 is now observable on the output O1), it creates a transition V(t) going from V5 to V6. It consequently appears that detection of the defect depends on the logic interpretation of this transition at time (t0+6Tcl):

- If V(t0+6Tcl) < Logic threshold of inverter 5 => N4 is interpreted as a faulty 0.
- If V(t0+6Tcl) > Logic threshold of inverter 5 => N4 is interpreted as a fault-free 1.

The value of V(t0+6Tcl) depends on the resistance of the open Rop, the capacitance of the faulty node C_N, the time (Tcl-Tpb), the polarity of the transition $P_{Vi-1/Vi}$, and the previous voltage V5=V(t0+5Tcl+Tpb). The voltage V5 itself depends on the same parameters and on the previous voltage V4=V(t0+4Tcl+Tpb), that depends on…. etc.

Finally, we give the following important property: 'Considering a test sequence of n vectors (T0…Tn) and a given test vector Ti for a resistive open on node Nj, the detection of the resistive open depends on the successive voltages V0, V1,…Vi-1 appearing of the faulty node through application of the sequence.

This small example clearly demonstrates that detection of a given resistive open does not depend on only one test vector. It depends on the whole set of vectors that have been applied to the circuit.

The smallest resistance that can be detected with this sequence is obviously not equal to the one given in the previous section. Due to the application of our 6 successive vectors, the minimum detectable resistance is equals to Rop^{min}=28KΩ.

4. Conclusion

This paper analyzes the electrical behavior of resistive open. It is important to note that the resistance of the open is an unpredictable parameter. The electrical behavior of the defect obviously depends on this random parameter as well as its detection conditions. It is demonstrated that the detection not only depends on the unpredictable resistance but also on the successive intermediate values of the faulty node voltage. Consequently, detection of such defect is not a matter of generating a single adequate vector but depends on all the vectors that has been previously applied to the circuit.

5. References

[1] R.Rodriguez-Montanes, P. Volf and J. Pineda de Gyvez, "Resistance characterization for weak open defects", IEEE Design & Test of Computers, Vol. 19, n°5, pp. 18-26, 2002.

[2] M. Renovell and G. Cambon, "Topology Dependence of Floating Gate Faults in MOS Integrated Circuits", Electronics Letters, Vol. 22, n°3, pp. 152-153, Jan. 1986.

[3] C.L. Henderson, J.M. Soden and C.F. Hawkins, "The Behavior and Testing Implications of CMOS IC Open Circuits", International Test Conf., pp. 302-303, 1991.

[4] S. Reddy, I. Pomeranz, T. Huaxing, S. Kajihara, S. Kinoshita, "On testing of Interconnect Open Defects in Combinational Logic Circuits with Stems of Large Fanout", International Test Conf., pp. 83-89, 2002.

[5] V.H. Champac, A. Zenteno, "Detectability Conditions for Interconnection Open Defects", IEEE VLSI Test Symposium, pp. 305-311, 2000.

[6] J.C.M. Li, C-W. Tseng and E.J. McCluskey, "Testing for Resistive Opens and Stuck Opens", International Test Conference, pp. 1049-1058, 2001.

[7] C.F. Hawkins et al., "Quiescent Power Supply Current Measurement of CMOS IC Detection", IEEE Trans. On Indust. Electr., Vol. 36, n°2, pp. 211-218, May 1989.

[8] H. Konuk, "Voltage and Current-based Fault Simulation for Interconnect Open Defects", Trans. On Computer-Aided Design of IC and Systems, Vol. 18, n°12, pp. 1768-1779, dec. 1999.

[9] H. Yan, A.D. Singh, "Experiments in Detecting Delay Faults using Multiple Higher Frequency Clocks and Results from Neighbouring die", International Test Conference, pp. 105-111, 2003.