TOWARDS DESIGNING A MULTISTANDARD SWITCHED-CURRENT ΣΔ MODULATOR IN 0.18μm, 1.8-V CMOS TECHNOLOGY

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ABSTRACT

Since the number of wireless standards has increased with the market communications growth, this paper deals the design of a 0.18μm, 1.8V switched-current ΣΔ modulator suitable for multistandard purposes. From transistor-level simulations we found a correct operation for GSM, Bluetooth, and WCDMA standards. The modulator is based on a reconfigurable switched-current ΣΔ architecture because of its programmability, compatibility with digital technologies and low-voltage operation. The deduced dynamic range/PC for this design was 12.0-b/57mW, 11.0-b/123mW and 7.8-b/156mW within 200kHz, 1.0MHz and 3.8MHz bandwidth, respectively.

1. INTRODUCTION

A great deal of attention has been devoted in open literature to the regulation of communications systems. The reason is simple, by one side the wireless communication industry is experiencing a personal communication services growth, which means multiple communications standards. On the other hand, because the complexity of modern circuits/devices/systems is due to its miniaturization, there are many EMC standards that must be harmonized. In a parallel way, while harmonized standards are actually under development [1] user enjoy/use services like image and video, voice, internet access, security, navigation and more. From the communications theory point-of-view these services are characterized by different communication standards; for example cellular phones and Wireless Local Area Networks (WLANs) include standards A={PCS, GSM, TDMA, CDMA, ….} and B={IEEE 802.11, Bluetooth ….}, respectively. If this communications environment is not enough, currently there is another wireless standard known as UWB [2] that is gaining popularity. In practice, the trend of the microelectronics industry is twofold:

- Develop an integrated system that provides multi-purpose functionality.
- Support much higher data rates at high link reliability and over greater distances.

In other words, the industry is looking for a system that takes advantage of the different services offered by co-existing technologies. Such a system would include both analog and digital circuitry and, very important, the final product must be low-cost and smaller than today radio transceivers. Figure 1 depicts a block diagram of a transceiver, where just the receiver architecture is shown for illustrative purposes [3]. Several analog blocks are needed including Analog-to-Digital Converters (ADCs) to digitize the signals.

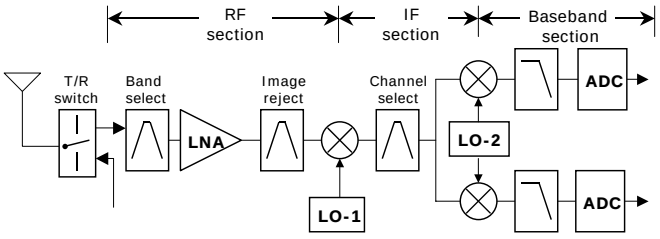


Figure 1. Basic architecture of the FDD/TDMA receiver.

The ADC is probably the most challenging building block for multistandard services because of the different sampling rates required for each individual operation mode. In addition, the bottled neck of multistandar systems is the lack of efficient high-resolution ADC. Analog components suffer from process, voltage and temperature variations, which have to be taken into account as an integral part of the design phase. In order to minimize

circuitry imperfections and obtain the required resolutions Sigma-Delta Modulators (ΣΔMs) appear as good candidates for designing ADCs. They have been implemented in either switched-capacitor or continuous time versions [4], [5]. However switched-current (SI) is an additional design option to design ΣΔMs because no analog components are needed. Furthermore, the basic building block is a current branch, which means that the signal is a current, thus the final design is a transistor-only development suitable for low-voltage operation.

The paper is described as follows. Section 2 presents a review of the modulator architecture, including an analysis of the SI basic memory cell. In section 3 additional design considerations deduced from HSPICE results are presented. At the end of the paper the conclusions are given.

2. RECONFIGURABLE ARCHITECTURE

It has been demonstrated that SI technique allows design circuits to be programmed and reconfigured [6]. The block diagram of the expandable cascade $2\text{-}1^P$ architecture is given in figure 2. It consists of a second-order first-stage followed by P first-order stages which can be connected or disconnected by the *control* circuitry according to the required noise-shaping. In addition, analog and digital coefficients are optimized according to the criteria described in [7]. The same is true for the memory cell, which can be reconfigured to achieve the modulator specs. In practice, because power dissipation increases as technology scales down, it is basic to determine how the various dissipation mechanisms scale.

From the design point-of-view programmability would be a procedure to minimize power dissipation. Here there are several design issues to take into account. As an example, design low ON-resistance for switches is mandatory even when area increases. Thus, deep-submicron technologies can be a design option because of its thinner gate oxide. In practice, designer faces daily design trade-offs. In that sense, this work uses technological parameters of a 0.18μm CMOS process and we are assuming that thermal noise is the dominant source of error. In consequence, the SNR that governs the performance of **L** basic memory cells is given by

$$\mathrm{SNR} = \mathrm{SNR}_{BC} + 10\,\mathbf{log(L)} \qquad (1)$$

where SNR_{BC} is the basic memory cell's signal-to-noise ratio. The second term represents the advantage of the **L** cells parallel connection. On the other hand, in order to analyze how increases the SNR without adding other error sources, we must take into account that SNR depends on the ratio $G=(I_{BIAS})^2/BW$, with I_{BIAS} being the basic memory cell bias current and BW the signal bandwidth (also called *channel spacing*). Then, we would propose a constant bias current and obtain the channel spacing for each standard. For instance 200kHz, 1MHz and 3.8MHz are needed for GSM, Bluetooth and WCDMA, respectively. Thus, according to (1) we should obtain a higher dynamic range SNR_{BC} for GSM and the lowest one for WCDMA. Other standards could be considered for illustrative purposes, i.e. IS-95 and IS-136 use a channel spacing of 30kHz. These standards require a resolution higher than GSM, which means that in-band error contributions like deflecting-setting must be taken into account. In other words eqn. (1) would be substituted by the correct design model. In this work we are assuming that eqn. (1) is the correct model to design a multistandard ΣΔ modulator, i.e. GSM, Bluetooth and WCDMA.

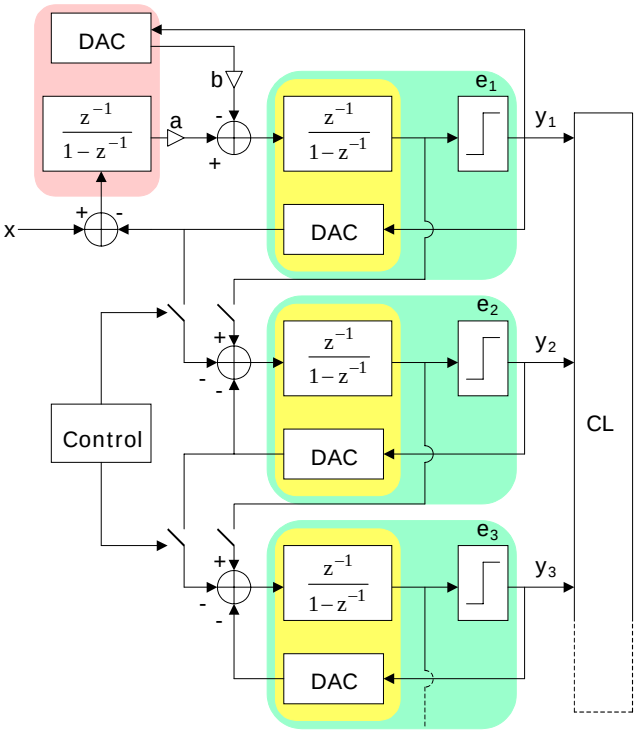


Figure 2. Reconfigurable $2\text{-}1^P$ ΣΔ modulator architecture.

As we have seen in figure 2, well-defined blocks compose the architecture and the same would be true for the layout design. The simplest block (SB) is that formed by both current integrator and 1-b DAC [6]. When SB is designed in conjunction with a comparator, we obtain a major block (MB) from which the design would be easier to include not only reconfigurability and programmability but also symmetry to minimize both systematic and random process variations.

Figure 3 shows the schematic of the integrator. It is composed basically by the cascade connection of two class AB memory cells and a unitary feedback loop. A third cell is used as the output stage. In order to reduce SI errors below 0.3% each memory cell includes a capacitor C_0 that is parallel connected with the memory transistor's gate-to-source capacitance, C_{gs1}. In practice SNR_{BC} is function of the memory cell's time constant

$$SNR_{BC} \propto \frac{G}{1 + t\frac{g_{mn1}}{C_{EX}}} \quad (2)$$

where **t** is the clock signal, $C_{EX}=C_{gs1}+C_0$ and g_{mn1} the transconductance of the memory transistor. Because the lower time constant the higher SNR_{BC}, that is the reason why C_0 was included in this design. Moreover, bias current (or equivalently g_{mn1}) should be as lower as possible to enhance the SNR_{BC}, however such design criteria is not completely true because G is negatively affected. Thus, we would conclude that SNR_{BC} is proportional to $(I_{BIAS})^{1.5}$, which is a trade-off to obtain higher resolutions because of the high power consumption. In this work our choice was C_{EX}>2.5pF and at least I_{BIAS}=1.0mA.

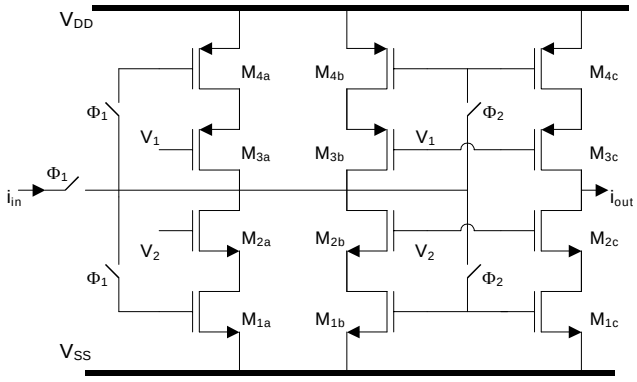


Figure 3. SI integrator. The clock frequency is 70.4MHz.

3. SIMULATION RESULTS

Figure 4 shows the design strategies to obtain the required resolution with SI errors below 0.3%. Taking into account power consumption, integration area and sampling frequency, our choice was the design strategy shown at the upper row. Electrical performance, deduced from HSPICE simulations, includes power consumption PC=123/156/57 mW, 11/7.8/12-b resolution, third harmonic distortion THD=-75/-77/-74dB for WCDMA, Bluetooth and GSM, with a switch ON-resistance lower than 100Ω. The same figure shows the output spectra of the modulator considering a half-scale input sinewave signal [6]. In this analysis the integrator's bias current was 1.5mA for Bluetooth because of the better performance, while for WCDMA and GSM a bias of 1mA was needed. As we can see, the sampling frequency is the same for the three standards.

Figure 5 shows the time domain simulation result of the proposed current integrator. Because the input signal is a 50μA step current the response increases 50μA per cycle (14.2ns) showing its correct operation. The same figure shows a summary of the current integrator's characteristics for each standard.

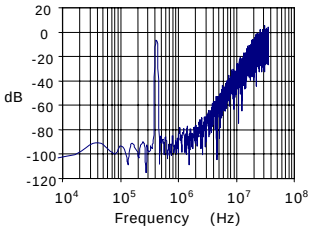
3.1 Where are we?

It is well known that power is being the bottleneck for the design of high performance modulators. By one side the power consumption obtained in this work is competitive according to that of other design techniques, however we must focus on minimizing the consumption by identifying firstly the various power dissipation components. Our results are based on the assumption that thermal noise is the dominant source of error. On the other hand, to the best of the authors' knowledge, the modulator proposed in this paper is the only one using SI circuit techniques intended for multistandard application. Indeed, we postulate that SI ΣΔ modulators are very promising from the point-of-view of frequency response, distortion, low-voltage operation and power consumption.

Bluetooth (11-b, 1MHz)

Modulator Order	Cells Number	Sampling (MHz)
2-1	3	70.4
$2\text{-}1^2$	2	40.0
$2\text{-}1^3$	2	26.0

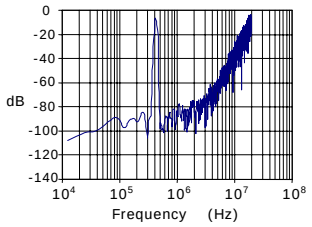
(a)



WCDMA (8-b, 3.8MHz)

Modulator Order	Cells Number	Sampling (MHz)
2-1	2	136.8
$2\text{-}1^2$	2	91.2
$2\text{-}1^3$	2	70.4

(b)



GSM (12-b, 200kHz)

Modulator Order	Cells Number	Sampling (MHz)
$2\text{-}1^0$	2	70.4
2-1	4	28.8
$2\text{-}1^2$	2	16.8

(c)

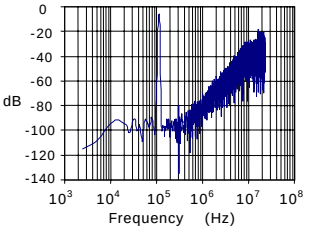
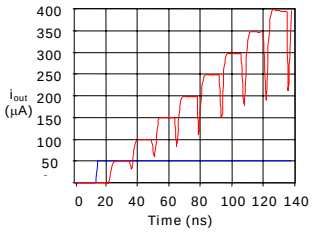


Figure 4. SI ΣΔ modulator characteristics and output spectra for the different standards.

Considering the factors mentioned above, Figure 6 shows the state of the art (FOM vs BW) of SI ADCs, where the proposed design is also included. Here, FOM is the figure-of-merit (the lowest the best) used to quantify the quality of ADC which is based on that proposed in [8]. It is basic to underline that figure 6 is a comparison between our design and those SI ADCs based on techniques different to ΣΔ. Note that the presented design gets the highest signal bandwidth reported to now for SI ΣΔ modulators. In addition, the design in this paper is a programmable architecture for multistandard applications, using modern deep-submicron technology, with moderate power consumption, thus allowing to take advantage of the different services offered by existing wireless technologies. Based on these considerations, if the

presented transistor-level electrical performance is confirmed by experimental results, the presented circuit will be at the cutting-edge of the state of the art on SI ΣΔMs.



SI integrator Clock frequency = 70.4MHz			
Parameter	Bluetooth	WCDMA	GSM
I_{BIAS}	1.5mA	1.0mA	1.0mA
g_m	6.0mS	4.0mS	4.0mS
R_{ON}	<100Ω	<100Ω	<100Ω
C_{EX}	3.9pF	2.6pF	2.6pF
ΣΔ modulator			
Power Cons	123mW	156mW	57mW
THD	-75dB	-77dB	-74dB
SNR	11-b	7.8-b	12-b

Figure 5. Step response of the SI integrator in HSPICE and ΣΔ modulator's electrical performance for each standard.

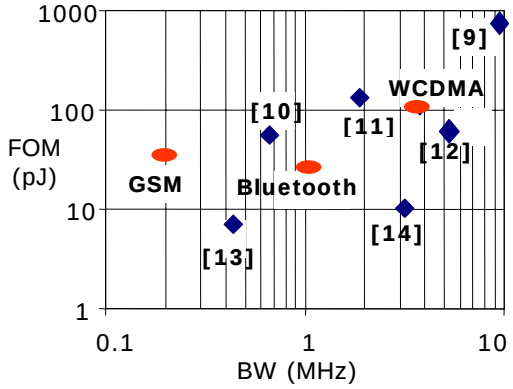


Figure 6. State of the art in SI ADCs.

4. CONCLUSIONS

Currently the communications industry is looking for a system that take advantage of the different services offered by co-existing technologies, i.e. image and video, internet access, security, navigation and more wireless services. Thus, that *system* not only must include multipurpose functionality but also be a low-cost and low-voltage solution. However, since the system includes analog and digital circuitry in this paper we are proposing the design of a SI ΣΔ modulator for designing the most challenging building block for multistandard services: the ADC. In this design approach the basic building block is a current branch, which means that signals are currents obtaining a transistor-only development suitable for low-voltage operation. To satisfy Bluetooth, WCDMA and GSM standards, we are proposing a modulator based on a configurable architecture. The deduced dynamic range, obtained from transistor level spice simulation, is under the assumption that thermal noise is the dominant source of error. In consequence the SI errors are below 0.3%. This design, sizing according technological design rules of a 0.18μm, 1.8V, CMOS process, features 12.0-b/57mW, 11.0-b/123mW and 7.8-b/156mW within 200kHz, 1.0MHz and 3.8MHz bandwidth, respectively. Future work includes the design of a test chip, fabrication and electrical characterization.

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5. REFERENCES

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