AUTOMATED TRANSISTOR SIZING METHODOLOGY FOR ANALOG CIRCUITS BASED ON SIMULATED ANNEALING AND COMPACT MODEL OF gm/I_D CHARACTERISTICS

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ABSTRACT

This paper presents a transistor sizing methodology for analog CMOS circuits that combines the physics-based gm/I_D characteristics provided by the ACM compact model and the simulated annealing technique for the circuit optimization. The methodology exploits different transistor widths and lengths and provides good solutions in a reasonable CPU time, with a single technology-dependent curve and accurate expressions for transconductance and current in all operation relgions. The advantage of constraining the optimization within a power budget is of great importance for the designer. As an example, we show the optimization results obtained for the design of a two-stage operational amplifier.

1. INTRODUCTION

The design of CMOS analog integrated circuits needs skilled specialists that often used detailed knowledge of the device technology and models to complete the design of blocks containing tens of transistors. The task is demanding due to the complex relations between the design objectives (multiple and complex performance specifications to be met, like bandwidth, gain, power, maximum offset voltage, power-supply rejection ratio, etc.) and the multiple design variables (transistor sizes and bias currents) to be set. Previous work has been done in the field of analog design automation to enable fast design at the block level. Different strategies and approaches have been used, such as spice simulation [12], symbolic simulation [6], artificial intelligence [4], manually derived design equations [3], hierarchy and topology selection [7] and geometric programming [8] [10]. The main difficulty encountered for widespread usage of these tools is that they require appropriate modeling of both devices (technology dependence) and circuit in order to achieve the design objectives in a reasonable processing time. The choice of different circuit topologies to support in a method or tool is also a problem, since most approaches work with topology-based equations, which limits the application range. The addition of new block topologies to the CAD system has to be supported, since it is a critical and often slow process that requires again expert designer knowledge. The use of optimization algorithms combined with design techniques seems to be a good solution when applied to specific applications, since a general solution most often proves to have shortcomings for fully exploiting the capabilities of the analog CMOS technology. The main requirements of an analog synthesis tool are: interactivity with the user, flexibility for multiple topologies and reasonable response time. The interface with an electrical simulator is also convenient.

This paper describes a methodology for analog design automation that combines the simulated annealing optimization technique, a physics-based transconductance-to-current ratio characteristics and the electrical simulation in the same environment, providing even to a non-expert user a very flexible tool that is able to size analog circuits including a broad range of constraints such as total power dissipation. The paper is organized as follows: Section 2 describes the proposed methodology and explains the relationship between the simulated annealing algorithm, the gm/I_D technique and the ACM MOSFET model; in Section 3 the synthesis of a two-stage operational amplifier is shown in order to demonstrate the capabilities of the methodology; finally, in Section 4 we present some conclusions.

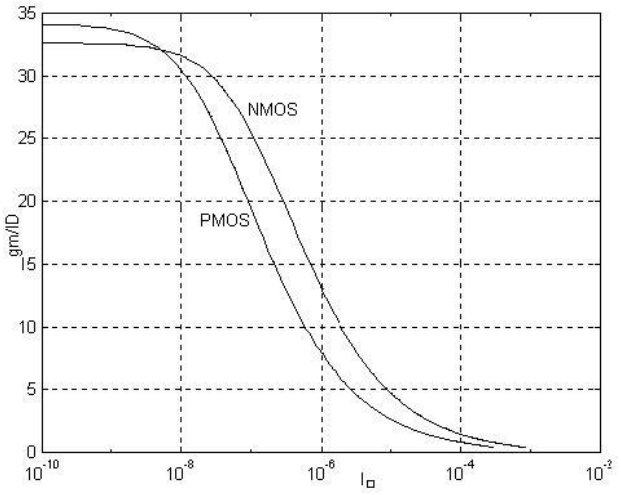

Fig. 1 – *gm/I*$_D$ x I curve for 0.35μm CMOS technology.

2. OPTIMIZATION METHODOLOGY

Simulated annealing (SA) is a well known random search technique which exploits an analogy between the way in which a metal cools and freezes into a minimum energy crystalline structure (the annealing process) and the search for a minimum of a cost function in a more general system. It forms the basis of an optimization technique for combinatorial and other problems [9]. The use of simulated annealing in the synthesis of analog circuits was reported in previous works [5][11]. SA's major advantage over other methods is the ability to avoid becoming trapped in local minima. The algorithm employs a random search which does not only accept solutions that decrease the objective cost function f_c (assuming a minimization problem), but also some changes that increase it. The latter are accepted with a probability

$$p = e^{-\frac{\Delta f_c}{T}} \quad (1)$$

where Δf_c is the increase in f_c and T is a control parameter, which by analogy to the annealing is known as the system "temperature" irrespective of the objective function involved. The analog circuit modeling for simulated annealing is straightforward. The design objective (e.g. minimum power and area) is called the cost function which has to be minimized and should be formulated appropriately. In this work we propose and use the following cost function:

$$f_c = \sum_{i=1}^{n} \beta_i \hat{p}_i(X) \quad (2)$$

where β_i is the weighting coefficient for performance parameter $\hat{p}_i(X)$ which is a normalized function of the vector of independent design parameters X. This function allows the designer to set the relative importance of competing performance parameters, such as, for example, a weighted relation between power and noise.

For the transistor sizing, knowledge-based equations that describe the relations between the transistors and specifications are needed. These equations are topology-specific and can be used within a synthesis methodology for the resolution of a system of non-linear equations. This system usually has more independent variables than equations, returning infinite solutions. If a set of design parameters has to be minimized, then the simulated annealing algorithm is a good option, since it exploits most of the design space, including different transistor lengths, which are kept fixed in most design tools.

For the circuit performance evaluation, we use a methodology called gm/I_D. The gm/I_D method considers the relationship between the ratio of the transconductance gm over DC drain current I_D and the normalized drain current $I_□ = I_D/(W/L)$ as a fundamental design tool [13], such as the curve shown in figure 1. The gm/I_D characteristic is related to the performance of analog circuits, gives a clear indication of the device operation region and provides a way for automating the calculation of transistors dimensions. The main advantage of this method is that only the gm/I_D x $I_□$ curve must be related to the fabrication technology parameters, a feature that facilitates the migration to another CMOS technology. In this work, the gm/I_D x $I_□$ curve is generated by electrical simulation using the ACM compact MOSFET model [2], which is also implemented in the commercial simulator SMASH. This model is composed by simple expressions to describe all regions of operation in a continuous representation of the transistor current and small-signal parameters.

The symmetry of the MOSFET drain-source is observed and a reduced number of model parameters is used. Moreover, all the parameters have a strong physical basis. The proposed methodology joins the SA algorithm, the gm/I_D technique and the ACM MOSFET model in the same environment in order to optimize the design of analog circuits based on the transistor inversion coefficient. The main advantage of using the SA over the crude gm/I_D technique is that the design space is explored in a more effective way, combining operation in weak and strong inversion to achieve optimum low-power design. Figure 2 shows the design flow. The user enters the design specifications, technology parameters and configures the cost function according to the required design objectives.

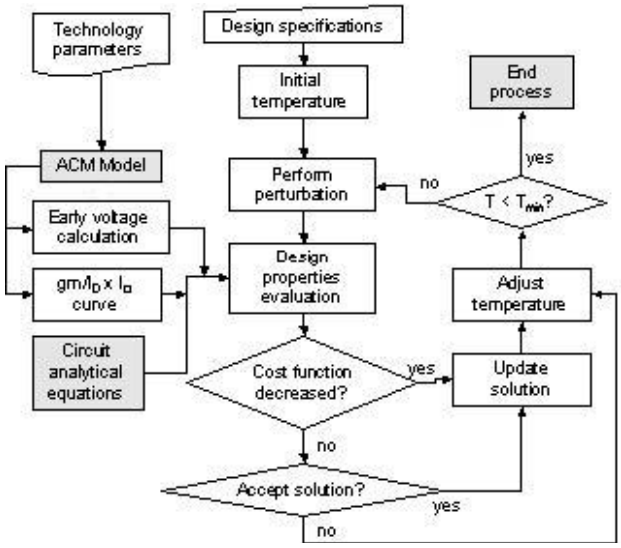

Fig. 2 – Proposed design flow

The optimization loop starts with a random perturbation on the design variables, whose amplitude is defined by the current temperature. These variables are defined by the user, and are always related to the transistor geometry, large and small-signal parameters, such as *W*, *L*, I_D, *gm* and gm/I_D. Following, the design properties evaluation is performed by the calculation of the circuit characteristics such as gain, cut-off frequency, phase margin, power, noise, etc. This is done using circuit specific analytical equations, the gm/I_D versus I_D curve and the ACM model for calculation of Early voltages, transconductances and currents. At this point, the cost function can be evaluated and the solution is accepted if the cost decreased or else if the cost increased with a probability given by equation 1. If the circuit is feasible, i.e., transistor sizes are within an allowed range, the new solution is accepted. Otherwise, it is discarded. The next iteration starts with a new temperature, which is calculated by

$$T_{k+1} = \alpha T_k \tag{3}$$

where α is a constant less than 1 and very close to this value. The index *k* indicates the iteration step. The process ends when the temperature achieves a minimum value or the variation in the cost function does not suffer relevant modification related to the perturbation in the variables. The temperature schedule can be configured through the choice of the α parameter in order to achieve the best relation between time response and solution refinement.

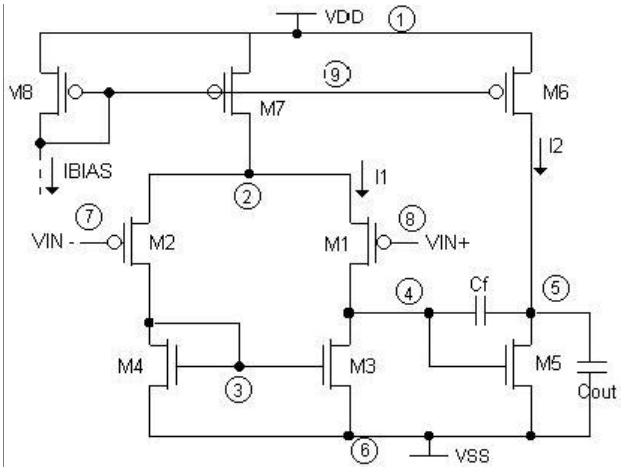

Fig. 3 – Schematics of a two-stage operational amplifier

Tab. 1 – Specifications and simulated results for the two-stage amplifier

Specification	Required	Simulated
Total current (μA)	≤ 200	102
Phase margin (°)	≥ 60	60
Low-frequency gain (dB)	≥ 90	95
GBW (MHz)	≥ 15	15
Slew-rate ($V/\mu s$)	≥ 15	15
$ICMR^-$ (V)	≤ -1	-0.8
$ICMR^+$ (V)	≥ 1	1.4
Total area (μm^2)	minimize	9064
Offset (μV)	≤ 200	160
Cost function	minimize	1.62

3. DESIGN EXAMPLE

The proposed design methodology was implemented in MATLAB and applied to the synthesis of a two-stage operational amplifier, shown in figure 3. This amplifier is composed by an input differential pair with active load in the first stage and an inverter amplifier in the second stage. A compensation capacitor is necessary for stability.

The analytical equations that describe the behavior of this circuit are well-known [1]. In this example, we want to size the transistors in order to achieve the design specifications given in Table 1. The design objective (f_c) is to minimize the relative area, low-frequency gain and total DC current in the following way:

$$f_c = \frac{A}{A_0} + \frac{I_{DD}}{I_{DD0}} + \frac{A_{v0}}{A_v} \tag{4}$$

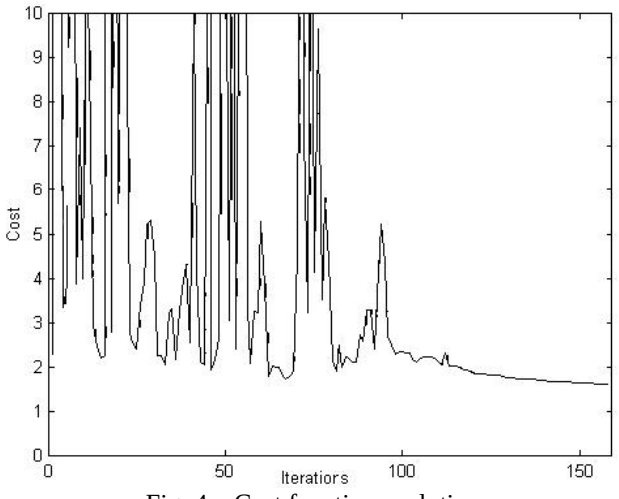

Fig. 4 – Cost function evolution

Tab. 2 – Transistor sizes obtained by the optimization procedure

Transistor	L (μm)	W (μm)	$gm/I_D(V^{-1})$
M1, M2	1.2	74.8	16.5
M3, M4	6.6	15	4.7
M5	0.6	147	15.7
M6	6	10.7	0.7
M7, M8	0.8	5.5	3.1

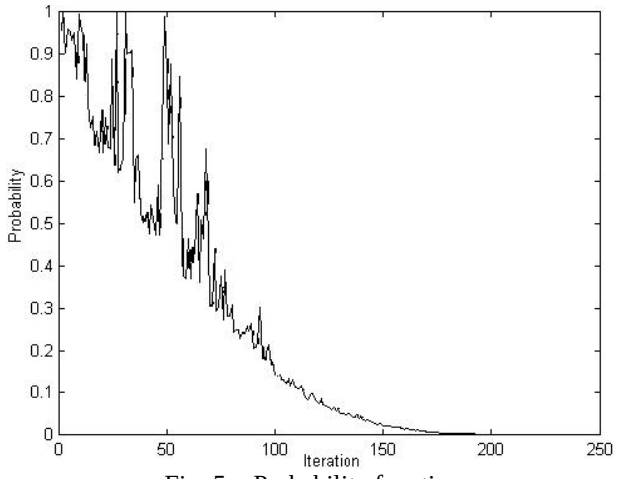

Fig. 5 – Probability function

Here, A is the silicon area occupied by all transistors, including drain and source regions (estimated), A_0 is a reference area for normalization, I_{DD} is the total consumed current and A_v is the low-frequency gain. The gate transconductance of the input differential pair is given by:

$$gm_1 = GBW \cdot C_f \tag{5}$$

The drain current for these transistors can be calculated with the information about the transconductance-to-current ratio, which is an independent variable:

$$I_{D1} = \frac{gm_1}{\left(\frac{gm}{I_D}\right)_1} \tag{6}$$

So, the aspect ratio for the input transistors is:

$$\left(\frac{W}{L}\right)_1 = \frac{I_{D1}}{I_{\square 1}} \tag{7}$$

$$W_1 = \left(\frac{W}{L}\right)_1 \cdot L_1 \tag{8}$$

where $I_{\square 1}$ is the normalized current given by the gm/I_D x I curve.

The same approach is done for the remaining transistors. For example, the size of the transistors in the current mirror load is:

$$\left(\frac{W}{L}\right)_3 = \frac{I_{D1}}{I_{\square 3}} \tag{9}$$

$$W_3 = \left(\frac{W}{L}\right)_3 \cdot L_3 \tag{10}$$

The design characteristics calculation is straightforward. The low-frequency gain is given by

$$A_v = \left(\frac{gm}{I_D}\right)_1 \cdot (VA_1 + VA_3) \cdot \left(\frac{gm}{I_D}\right)_5 \cdot (VA_5 + VA_6) \tag{11}$$

The Early voltage VA is estimated using the ACM model according to the transistor length. In this example, the technology used is 0.35µm CMOS, the power supply voltage is ±1.65V and the load capacitance is 10pF. The independent variables subjected to perturbations by the simulated annealing algorithm are: $L_1 = L_2$, $L_3 = L_4$, L_5, L_6, L_7, $\left(\frac{gm}{I_D}\right)_1 = \left(\frac{gm}{I_D}\right)_2$, $\left(\frac{gm}{I_D}\right)_3 = \left(\frac{gm}{I_D}\right)_4$, $\left(\frac{gm}{I_D}\right)_5$, $\left(\frac{gm}{I_D}\right)_6$, $\left(\frac{gm}{I_D}\right)_7$, and the dependent parameters are $W_1 = W_2$, $W_3 = W_4$, W_5, W_6, $W_7 = W_8$, C_f and bias current. The conditions $L > L_{min}$, $W > W_{min}$ and

$\left(\frac{gm}{I_D}\right)_{\min} \leq \left(\frac{gm}{I_D}\right) \leq \left(\frac{gm}{I_D}\right)_{\max}$ avoid infeasible solutions, with L_{min} = 0.3µm, W_{min} = 0.6µm, $(gm/I_D)_{min}$ = 0.1 and $(gm/I_D)_{max}$ = 25.

The optimization process for the example took 158 iterations and 91 million floating point operations. The final transistors sizes obtained by the iterations with the analytical models are shown in table 2. The second column of table 1 shows the performance of the optimized solution, as estimated by electrical simulations with SMASH. Figure 4 shows the evolution of the cost function. We can note the convergence of the cost function to a minimum value, stabilizing when the temperature freezes. In figure 5 is shown the probability function, which decreases as the number of iterations increase. A probability of 1 indicates that a worse solution is accepted with 100% of chance.

4. CONCLUSION

In this work we presented a sizing method that combines simulated annealing algorithm, the gm/I_D technique and the ACM MOSFET model in the same environment. The proposed methodology exploits different transistor lengths and provides an acceptable solution in a reasonable CPU time. The main advantage is the simple sizing method based on the transistor inversion coefficient, which is calculated by a single technology-specific characteristic curve gm/I_D versus I . The design space is not limited to strong inversion region, but also to moderate and weak inversion, allowing low-power optimum design. The disadvantage is the necessity of fixed-topology analytical equations, which suggests that the next development is the support the tool has to provide to a library of analog blocks of common circuit topologies.

5. REFERENCES

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