AN ACOUSTIC SURVEILLANCE UNIT FOR ENERGY AWARE SENSOR NETWORKS: CONSTRUCTION AND EXPERIMENTAL RESULTS

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ABSTRACT

This paper presents an acoustic surveillance unit (ASU) built in the framework of a project for the localization of audio sources. The unit is targeted to locate vehicles emitting sounds in the range [10Hz-300Hz] with an accuracy of one degree. Experimental results for the unit, measured in an outdoor environment are shown.

1. INTRODUCTION

This paper presents an acoustic surveillance unit (ASU) built in the framework of a project for the localization of audio sources. The unit is targeted to locate vehicles emitting sounds in the range [10Hz-300Hz] with an accuracy of one degree. The method used to locate the targets is based on a modification of the correlation of the signals captured by two microphones ([1], [2]). Actually, as described originally in [7], the method proposed performs a derivative on the correlation of inputs, which at the same time reduces the size and the power consumption of the resulting integrated circuit (IC) realization [6].

Increased attention has been paid lately to the topic of acoustic localization, especially from the point of view of energy aware sensor networks [3][4], which calls for low power electronic implementations. Several methods have been presented in the literature including IC realizations for this task (see [8]-[14]).

The ASU reported in this paper is composed of an acoustic enclosure of 11cm of diameter, four miniature microphones in quadrature, four-channel discrete electronic preamplifiers and comparators, two cascadable correlation-derivative IC's [6], and a radiofrecuency interface to communicate the data. Details of the unit, as well as the results of the unit testing in an outdoor environment are reported.

P. Julián is also with CONICET.

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2. NODE DESCRIPTION

In this section, we describe every part of the acoustic surveillance unit (ASU) node, which is formed mainly by an acoustic enclosure, a signal conditioning circuitry, a process unit and finally a MICA2[1] interface. The figure 1 shows a scheme of the node.

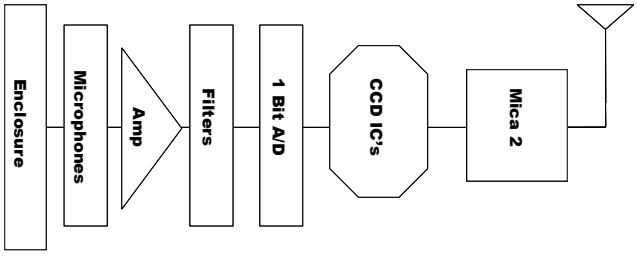

Figure 1. Node parts

2.1 Acoustic enclosure

The acoustic enclosure has an array of four Knowless Sysonic MEMS microphones. This enclosure produces an effective separation between microphones larger than the actual microphone separation, which is 6cm. The enclosure diameter is 11cm, and its height is 3cm. The microphones exhibit a sensitivity of -22dB and a noise level of 35dbA sound pressure level (SPL). They also have an internal amplifier with a maximun variable gain of 20dB.

2.2 Signal conditioning circuitry

The signal conditioning circuitry is formed by an amplifying/filtering stage and a 1 bit analog to digital (A/D) converter for each microphone. The amplification stage was designed in order to amplify the milivolt level input signal into a volt level signal. This stage also acts as a filter, to limit the input signal bandwidth to the range [10 - 400] Hz. The 1 bit A/D stage is a comparator that clips the signal and produces a digital output that goes to the process unit.

[1] MICA2 is the name of sensor node fabricated by CrossBow Technology Inc. http://www.xbow.com

Amplifiers, filters and comparators were implemented using commercial-off-the-shelf (COTS) components. Because the cross-correlator estimator depends directly on the phase difference of the incoming signals, particular care was taken in the selection of the components to minimize the mismatch between the channels. In particular, the frequency response was set with a phase mismatch lower than 0.3 σ [5]. In Fig.2 we show the analogic circuits and the microphone schematics.

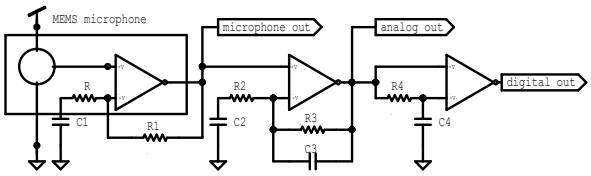

Figure 2. Signal conditioning circuitry and microphone schematic

2.3 Process unit

The process unit has two cascadable cross-correlator ICs, a 400 KHz clock unit, an 8 bit latch for the data bus and standard logic to multiplex the digital signals form the A/D converters to the cross-correlator ICs.

The cross-correlator IC is a modified and improved version of a previously presented design [6], which had 10 bits precision, a built-in state machine, a fixed range of measurement (given by 104 delay stages) and a fixed time integration window of one second. The new design exhibits lower power consumption, more precision (11 bits), and an increased flexibility given by the possibility of: a) cascading several units for extended range of measurement, or for a fixed range of measurement but different operation frequencies, allowing variable precision; b) controlling the integration time window externally.

The circuit has 64 cross-correlator-derivative stages as described in [6], where each one has a signed 10 bit UP/DOWN counter. Two signals are input to the unit, one of them, namely Din, is delayed internally and fed to the correlator while the other, namely Nin, is also fed to the correlator but without delay. The unit detects when Din is ahead of Nin by a time delay between 0 and 64 times the internal clock period, which doubles the external.

In order to explain the structure of this block, we will assume that signal X1 (fed across Din) is delayed with respect to X2 (fed across Nin).

Signal X1 is fed in a delay chain consisting of 64 D flip-flops (FF). Associated to each FF there is one stage, based on a 10 bit UP/DN signed counter, that produces the derivative of the correlation function. This structure is shown in Fig. 3.

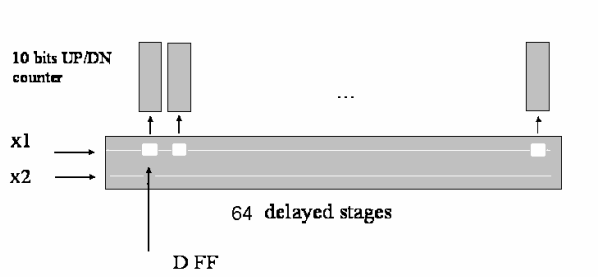

Figure 3. Block to measure the delay of X1with repect to X2

The i-th stage computes the following operation:

$$DC(i) = \sum \big(X_1(t-i)X_1(t-i-1)\big)X_2(t) \quad (1)$$

It can be easily seen that the discrete set of values DC(1) DC(2) …. DC(64) is the discrete derivative of the set of values C(1) C(2) …. C(64) that would be obtained if the correlation were evaluated.

$$C(i) = \sum X_1(t-i)X_2(t) \quad (2)$$

To achieve good power efficiency, the calculation of DC is done as follows: An auxiliary block, called signal generator, generates two signals UP and DN. If X1 is leading with respect to X2 then the UP signal will be 1 as long as X2 is 1. If X2 is leading with respect to X1 then the DN signal will be 1 as long as X2 is 1. In addition, two new clock signals are created. In figure 4 we show an example of the signals involved.

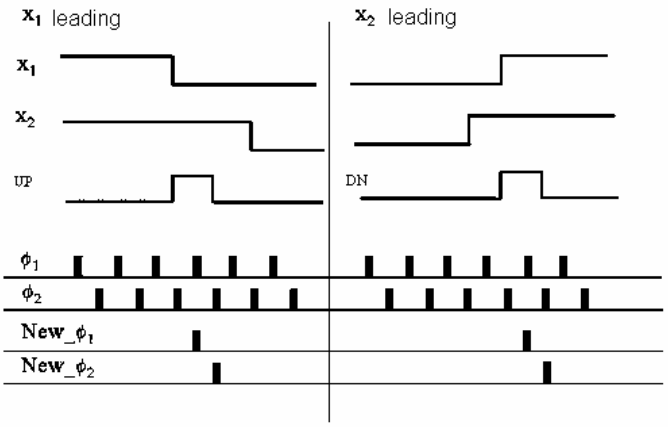

Figure 4. Generation of signals UP and DN and the new (two-phase) clock.

The UP and DN signals together with the new clock signals, are then fed to a synchronous 10 bit UP/DN counter.

The output of this block is the most significant bit (11th bit), which is also the bit that defines the sign of the count. At the beginning of each measuring cycle the count is reset to zero. As we want to detect the zero-crossing, we need to find a change from 0 to 1 or from 1 to 0 in the output bit of two consecutive UP/DN counters. This is done using XNOR gates.

The last step is to encode the position of the location where the zero-crossing has been found to a binary number. This is done connecting the output of the XNOR gates to an array of 8-3 lines Priority Encoders. Every encoder in the first layer takes 8 outputs from the XNOR gates and sends the output to another layer of encoders. These two layers provide the 6 bits output. These bits are wired into a common bus, which can be done thanks to the three-state output of the encoders. Figure 5 shown a block diagram of the internal structure of the IC.

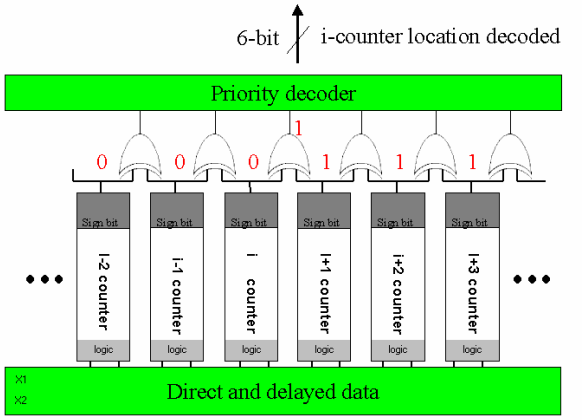

Figure 5. Internal structure of the cross-correlator IC

In addition, the encoders have Input/Output Enable signals that permit to set the priority in case two events (zero crossings) are detected simultaneously. The priorities are set in such a way that the stages with less delay have more priority.

The IC was fabricated in a 0.5µm standard CMOS process, and has 64 stages with a power consumption per delay stage of 0.77µW (at 3.3V and 200Khz). In the case under study, two IC's were used and every stage has a 5µs delay; therefore, the total range of the setup is 640µs. Table I summarizes the power consumption of one cross-correlator IC.

TABLE I. CROSS-CORRELATOR IC POWER CONSUMPTION (AT 3.3V)

Description	*Power*
Cross-correlator	45.7 uW
Internal reset generator	6.2 uW
Pads	10.3 uW
Total	**62.2 uW**

Recent results indicate that the chips work correctly at 2V with a power consumption of 12µW.

Table II summarizes the most important static power consumption in the ASU unit (without the MICA2), including all integrated and discrete parts. There were measured at Vcc = 3.3 V, without input signal activity.

TABLE II. ASU STATIC CONSUMPTION ASU STATIC CONSUMPTION

No.	*Description*	*Current*	*Power*
4	MEMS microphone	850 uA	2805 uW
4	TLV2382	28 uA	93 uW
4	Lmx393	160 uA	528 uW
2	74hc4049 (clock generator)	100 uA	330 uW
2	Cross-correlator IC	38 uA	125 uW
	Total	1176	3880 uW

2.4 MICA2

A Crossbow's MICA2 unit is used to control the input data multiplexing, in order to acquire output data from the cross-correlator IC bus, and to send the bearing estimation to the other nodes in the network.

3. TEST AND EXPERIMENTAL RESULTS

Experimental results were collected in a field test in an open area outdoors Bahia Blanca city. The ASU was located in the center of a field, and a speaker was placed 15 m away. Figure 6 shows the location of the ASU, the speaker and the measured angles. Three different sets of data were collected. The first set of data corresponds to angles in the range [0º-180º] in steps of 10º; the second and third sets of data correspond to angles in the range [1º-9º] and [85º-95º] in steps of 1º (see Fig. 7).

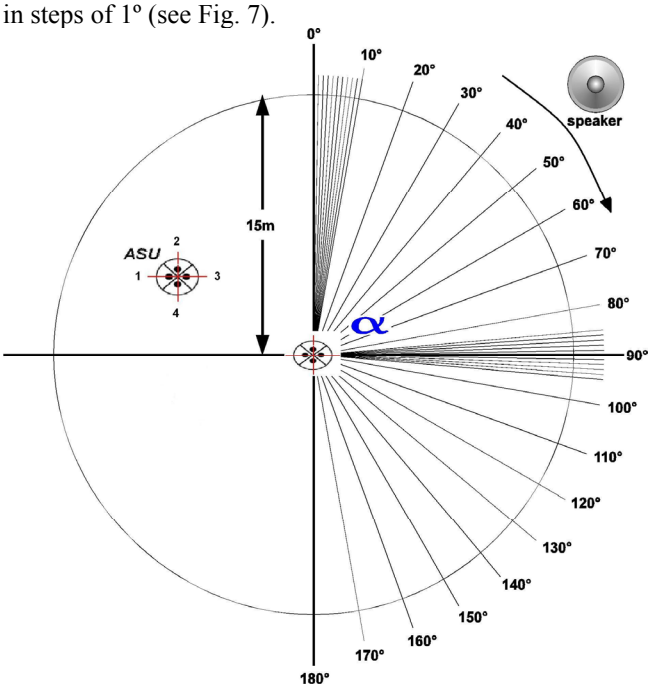

Figure 6. Test setup

A 200 Hz sine tone signal was played through the speaker and the signal received at the four microphones was recorded using a 10 KHz sampling frequency. The sound pressure measured at the ASU was 67 dbA. For every reference angle, we played 30s of signal and obtained 11

different readings of time delay from the process unit for each pair of microphones. The window time for each combination of microphones was 0.65s, resulting in a complete reading cycle of 2.6 s. The sequence of microphone pairs was 1-3, 2-4, 3-1, 4-2.

After the experiment, the analog signals recorded after the preamplifiers were used to simulate the ideal response of the cross-correlation derivative (CCD) algorithm. The idea behind this was to compare the results of the ideal algorithm and the data obtained from the real chip, after filtering and the one bit A/D conversion.

Figure 7 shows the time delay versus angle for three valid combinations in the range [0º-180º].

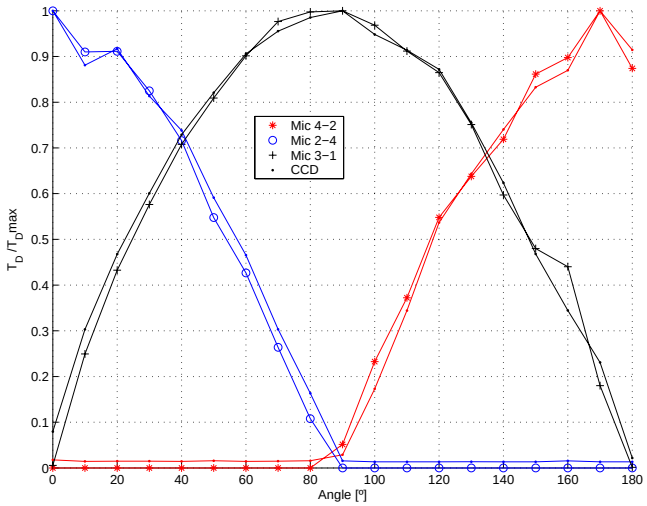

Figure 7. Time delay versus microphones combination

We used the measured and calculated delay to estimate the effective separation of the microphones in the ASU. We choose the mean value of delay in the range [80º-100º] for the microphone combination that gives the maximum delay in order to minimize errors [6]. Figure 8 shows the variation of effective separation. Table III presents the average effective separation in both ranges. These values were used in the calculation of the bearing angle.

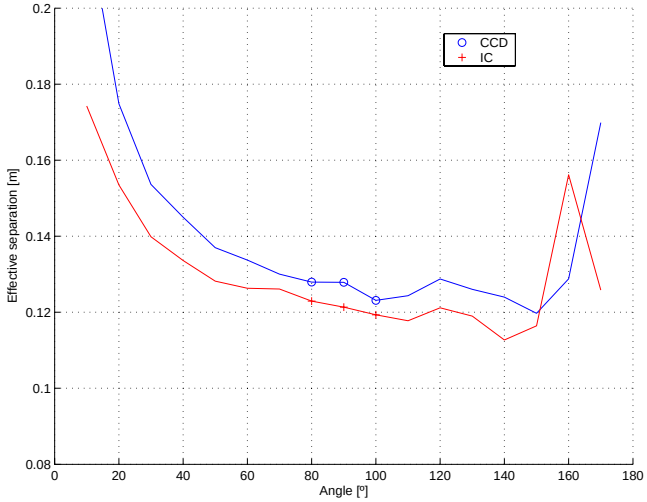

Figure 8. Microhopnes effective separation

TABLE III. MICROPHONES EFFECTIVE SEPARATION

Range	***[10 º-170º]***	***[80º-100º]***
CCD	14.10cm	12.63cm
IC	13.03cm	12.11cm

For every angle, the mean was used to define the characteristic of calculated angle versus reference angle, and the standard deviation was used to quantify the precision. Both, mean and standard deviation are shown in fig. 9 and 10 for the range [0º-180º] and figs. 11 and 12 for the range [85º-95º].

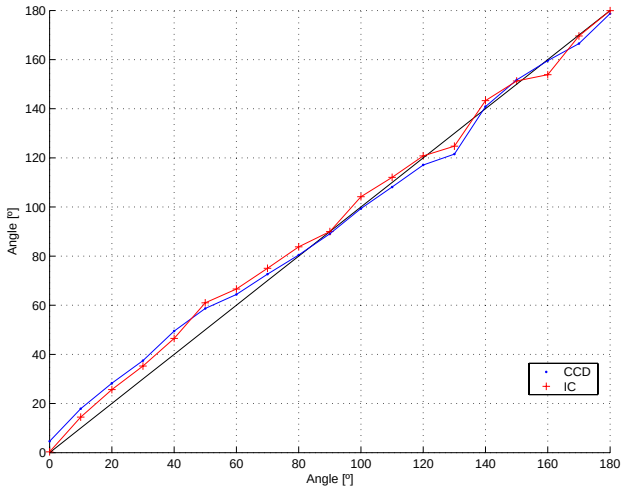

Figure 9. Estimated angle versus reference angle in the range [0º - 180º]

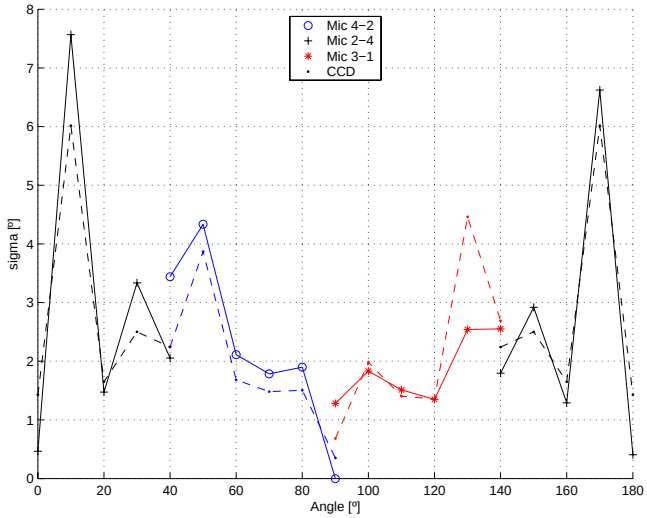

Figure 10. Standard deviation versus reference angle in the range [0º-180º]

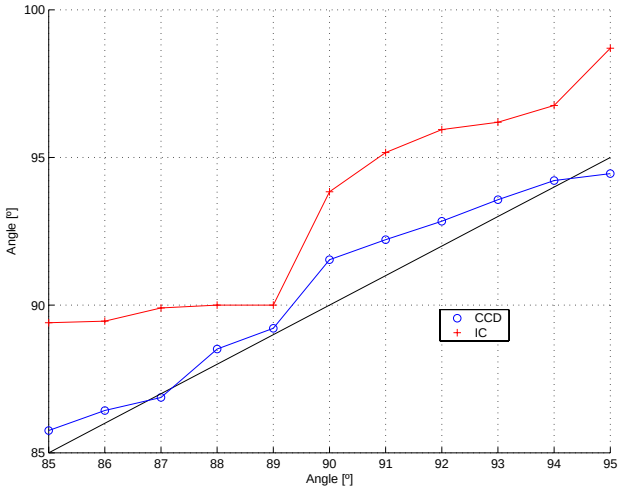

Figure 11. Estimated angle versus reference angle in the range [85º-95º]

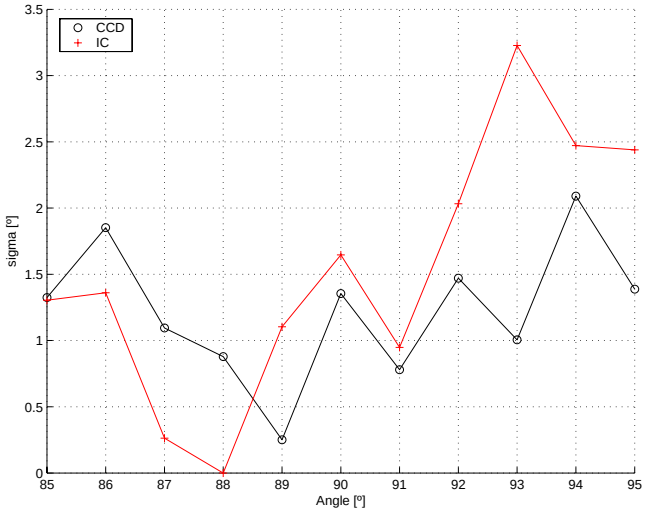

Figure 12. Standard deviation versus reference angle in the range [85º-95º]

Table IV and table V summarizes the average standard deviation of the two approaches in different ranges. Table VI shows the absolute value of the difference between the simulated and measured data, in different ranges.

Range	***[0º - 40º]***	***[40º - 90º]***	***[90º - 140º]***	***[140º - 180º]***	***[0º - 180º]***
CCD	2.77º	1.85º	2.10º	4.96º	2.92º
IC	2.98º	2.26º	1.84º	4.89º	2.99º

TABLE IV. ACCURACY OF IMPLEMENTATION (MEAN STD) IN DEGR EES

Range	***[1 º - 9º]***	***[85º - 95º]***
CCD	1.07º	1.23º
IC	1.53º	2.63º

TABLE V. ACCURACY OF IMPLEMENTATION (MEAN STD) IN DEGREES

Range	***[0º - 40º]***	***[40º - 90º]***	***[90º - 140º]***	***[140º - 180º]***	***[0º - 180º]***	***[1 º - 9º]***	***[85º - 95º]***
| CCD – IC |	0.21	0.41	0.26	0.07	0.07	0.46.	1.3

TABLE VI. ABSOLUTE VALUE OF DIFERENCE BETWEEN ACCURACY OF IMPLEMENTATION (MEAN STD) IN DEGREES

The standard deviation of measurements and calculated bearing angles are greater than 5° in some particular points of the range (10° and 170°), and for the rest of the range, close to 3º. Even though the differences between field measurements and angles calculated using a MatLab implementation of the derivative cross correlation algorithm are not greater than 1º. From this fact we can infer that the standard deviation is produced by noisy input signals. The differences between standard deviation and its mean are shown in Fig. 13.

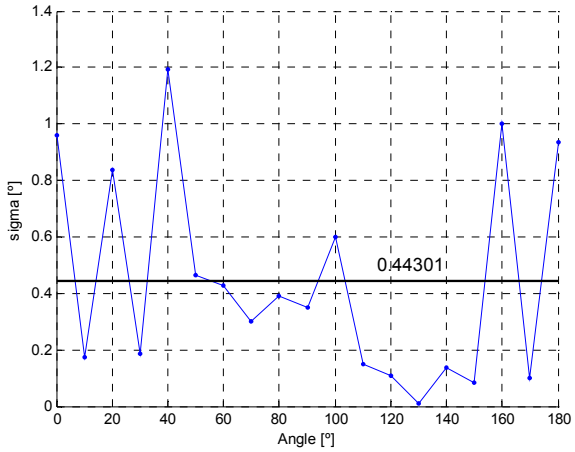

Figure 13. Standard deviation difference versus reference angle in the range [0º - 180º]

4. CONCLUSIONS

Test results for an ASU that performs bearing estimation have been presented. The unit is intended to work as a node in a sensor of network. The construction has been done using a low power IC specifically designed for the problem, low power off the shelf components and a Mica2 station for wireless communication. Accuracy comparison between field data and simulation results have been made in three different angle ranges, showing good matching between the real implementation and the ideal case.

7. REFERENCES

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