ANALYSIS OF THE START POINT AND DESIGN TRAJECTORIES FOR MINIMAL TIME SYSTEM DESIGN

Alexander Zemliak

Puebla Autonomous University

azemliak@fcfm.buap.mx

ABSTRACT

The set of the different design strategies for analog system design was analyzed on the basis of the new system design methodology. Optimal position for the design algorithm start point was analyzed to minimize the computer design time. The initial point selection has been done on the basis of the before discovered acceleration effect of the system design process. The geometrical dividing surface was defined and analyzed to obtain the optimal position of the algorithm start point. Numerical results of both passive and active nonlinear electronic circuit design prove the possibility of the optimal selection of the design algorithm start point.

1. INTRODUCTION

The problem of the computer time reduction of a large system design is one of the essential problems of the total quality design improvement. Besides the traditionally used ideas of sparse matrix techniques and decomposition techniques [1]-[6] some another ways were determine to reduce the total computer design time.

Another formulation of the circuit optimization problem was developed in heuristic level some decades ago [7]. This idea was based on the Kirchhoff laws ignoring for all the circuit or for the circuit part. The special cost function is minimized instead of the circuit equation solving. This idea was developed in practical aspect for the microwave circuit optimization [8] and for the synthesis of high-performance analog circuits [9] in extremely case, when the total system model was eliminated. The last idea that excludes the Kirchhoff laws can be named as the modified traditional design strategy (MTDS).

The generalized theory for the system design on the basis of the control theory formulation was elaborated in some previous works [10]-[11]. This approach serves for the time -optimal design algorithm definition. On the other hand this approach gives the possibility to analyze with a

great clearness the design process while moving along the trajectory curve into the design space. A general methodology we named the General Design Strategy (GDS). It includes a set of the different design strategies. The traditional design methodology, that we call Traditional Design Strategy (TDS), and the MTDS are two extreme cases of the GDS, when all the circuit model equations are solved during the design process (TDS) or all the circuit equations are eliminated from the circuit model during the design process (MTDS). It is necessary to introduce the special penalty function for the MTDS [10]. The optimization procedure in this case is realized in broadened optimization space, but as described in [12] for the complex system synthesis a significant computer time gain can be obtained. The GDS combine all the possibilities using some equations in the system representation as in TDS and some of the so call penalty functions in the objective function as in MTDS. Such possibilities are selected by means of the control function vector U [10], the result is 2^{M} possible design strategies, where M is the number of the system dependent parameters.

The use of GDS allows the appearances of the acceleration effect [13]-[14], as consequence the total computer time diminish, however such effect is highly dependent of initial values for the design process. In order to construct an optimal algorithm for the design process it is necessary to characterize the behavior of the design trajectories and therefore of the time consumption, according to the start point and give a rule for the automatic selection of better initial values. The present work is intended to answer some of the questions associated with the selection of initial conditions needed in the quasi optimal algorithm for design process.

This paper is organized as follows: in section 2 the necessary definitions are made; section 3 is devoted to the separate surface analysis, which is divided in two subsections, one for passive circuits and other one for active circuits; finally conclusions are made in section 4.

2. PROBLEM FORMULATION

We divide the vector of the system state variables X into two parts: the vector of the independent variables X', $X'=(x_1, x_2, ..., x_K)$, where K is the total number of independent design variables and the vector of the dependent variables X'', $X''=(x_{K+1}, x_{K+2}, ..., x_{K+M})$ where M is the total number of dependent design variables.

The design process for any analog system design can be defined [10] as the problem of the generalized objective function F(X, U) minimization by means of the vector equation (1) with the constraints (2):

$$X^{s+1} = X^s + t_s \cdot H^s \tag{1}$$

$$(1 - u_j)g_j(X) = 0, \quad j = 1, 2, \dots, M$$
 (2)

where $X \in \mathbb{R}^N$, X = (X', X''), $X' \in \mathbb{R}^K$ is the vector of the independent variables and the vector $X'' \in \mathbb{R}^M$ is the vector of dependent variables (N = K + M), $g_j(X)$ for all *j* is the system model, *s* is the iterations number, t_s is the iteration parameter, $t_s \in \mathbb{R}^1$, H = H(X, U) is the direction of the generalized objective function F(X, U)decreasing, *U* is the vector of the special control functions $U = (u_1, u_2, ..., u_m)$, where $u_j \in \Omega$; $\Omega = \{0;1\}$. The generalized objective function F(X,U) is defined as: $F(X,U) = C(X) + \mathbf{y}(X,U)$ where C(X) is the ordinary design process cost function, and $\mathbf{y}(X, U)$ is the additional penalty function: $\mathbf{y}(X, U) = \frac{1}{e} \sum_{j=1}^{M} u_j \cdot g_j^2(X)$.

This problem formulation permits to redistribute the computer time expense between the problem (2) solve and the optimization procedure (1) for the function F(X,U). The control vector U is the main tool for the redistribution process in this case. Practically an infinite number of the different design strategies are produced because the vector U depends on the optimization procedure current step. The problem of the optimal design strategy search is formulated now as the typical problem for the functional minimization of the control theory. The functional that needs to minimize is the total CPU time T of the design process. This functional depends directly on the operations number and on the design trajectory that has been realized. The main difficulty of this problem definition is unknown optimal dependencies of all control functions u_j .

3. TRAJECTORY ANALYS IS

The acceleration effect of the design process has strong dependency from initial point selection [13]; it may not appear under certain circumstances. How we can achieve the acceleration effect by means of the initial point variation? To answer this question a non conclusive but extensive study, for passive and active circuits, has been done in [14]. A systematic idea for selecting initial values is a geometrical one, and it is based on the conception of the Separate Surface, which is defined as the surface that divides the total design space in two subspaces. The first subspace includes all points that can produce the acceleration effect and the second subspace defines the points that can not be used for the acceleration effect obtaining.

The shape of Separate Surface represents the behavior of the design process according to the start point, and it is different for different type of circuits, for that reason the study of separate surface made here is divided in passive circuits and active circuits.

3.1. Passive circuits separate surface

Analysis of separate surface for passive circuits of different nodes is presented in this section for linear and non linear examples. The description for the design process is made briefly in each example; the complete emphasis is put on results related with the separate surface concept. The problem of the initial point selection for the design process is one of the essential problems of the timeoptimal algorithm construction.

3.1.1. Example 1

The analysis of the design process and acceleration effect for the simplest electronic circuit (2-dimensional problem) of the Fig. 1 was provided in [14]. The vector of the state variables X has two components $X = (x_1, x_2)$ where $x_1^2 = R_1$, $x_2 = V_1$. The nonlinear element has the following dependency: $R_n = r_0 + bV_1$. The function g(X) is described by the Laws of Kirchhoff:

$$g_1(X) \equiv (x_1^2 + r_0 + bx_2)x_2 - x_1^2 = 0 \qquad (3)$$

The objective function is defined by the formula $C(X) = (x_2 - k_v)^2$, where k_v has the fixed value. There is only one control function u_1 in this case because there is only one dependent parameter x_2 . The design trajectory for this example is the curve in two-dimensional space, if the numerical design algorithm is applied.

The optimization procedure and the electronic system model, in accordance with the new design methodology



Figure 1. Simplest one node circuit.

[10], are defined by the next two equations:

$$x_{i}^{s+1} = x_{i}^{s} + t_{s} \cdot f_{i}(X, U), \quad i = 1,2$$
 (4)

$$(1-u_1)g_1(X) = 0$$
 (5)

where U is the vector of control variables, and the components of the movement directions $f_i(X,U)$ for the i=1,2 depend on the optimization method.

These functions, for the gradient method for example, are given by the formulas:

$$f_1(X,U) = -\frac{d}{dx_1} F(X,U)$$
(6)

$$f_{2}(X,U) = -u_{1}\frac{d}{dx_{2}}F(X,U) + \frac{(1-u_{1})}{t_{s}}\left[-x_{2}^{s} + h_{2}(X)\right]$$
(6')

where F(X, U) is the generalized objective function, $F(X, U) = C(X) + \frac{1}{e}u_1g_1^2(X)$, $h_2(X)$ is the implicit function $(x_2^{s+1} = h_2(X))$ and it gives the value of the parameter x_2 from the equation (5), and the operator $\frac{d}{dx_i}$ for i=1,2 means: $d = \frac{\partial F}{\partial F} + \frac{\partial F}{\partial x_2} - \frac{d}{\partial F} = \frac{\partial F}{\partial F}$

$$\frac{\mathbf{d}}{\mathbf{d}x_1}F = \frac{\partial T}{\partial x_1} + \frac{\partial T}{\partial x_2}\frac{\partial x_2}{\partial x_1}, \quad \frac{\mathbf{d}}{\mathbf{d}x_2}F = \frac{\partial T}{\partial x_2}$$

As shown in [14] we need to select the initial point of the design process with the negative coordinate x_2 for this circuit. In this case the acceleration process can be realized. The more complicated circuit analysis shown that the start point selection with at least one negative initial coordinate of the vector X and the value of this coordinate that gives the start point position under the special separate



Figure 2. MTDS family curves in plane x_1 - x_2 for onenode circuit.

line are the sufficient conditions for the acceleration effect appearance. The more detail analysis shows that the negative value of the start point coordinate below the separate line is the sufficient condition for the acceleration effect but it is not the necessary. The phase diagram of Fig. 2 that corresponds to the above mentioned circuit includes two types of the separate lines. The first line AFB separates the trajectories that draw to the final point F from the left and from the right. The second separate line CTFB divides all the phase space to the two subspaces. All the points and trajectories that lie inside this separate line can not produce the acceleration effect. On the other hand, all the points that lie outside the separate line and corresponding trajectories produce the acceleration effect. These geometrical conditions are the necessary and sufficient to obtain the acceleration effect. The Ndimensional case has been analyzed below.

3.1.2. Example 2

This example corresponds to the five cells passive circuit and it is used to analyze the separate surfaces for the passive circuits from 2 to 5 nodes (Fig. 3). The design process is defined by the equations (1)-(2).

We begin our analysis for this example with two first cells of Fig. 3 as a result of design process the different design trajectories are obtained. Fig. 4 (a) shows a projection of separate surface type 1 (PSS 1), which is composed by two actually possible design trajectories.

There are three independent variables fixed to 1, $x_1^0 = x_2^0 = x_3^0 = 1.0$ and two dependent variables $x_4^0 = 1.0$ and $x_5^0 = x_t^0$, where x_t is the "tracer" variable which value variations is used to obtain the MTDS family curves, in order to know the separate surface behavior. There is a non linear element, $y_{n1} = r_0 + b_{n1}(x_5 - x_4)^2$ with $b_{n1} = 1$ (non linear



Figure 3. Five cells passive circuit with four non linear elements y_{ni} .





case). From Fig. 4 (a) it is possible to say that acceleration effect is presented when $|x_5^0| > 0.38$ for $x_1^0 = x_2^0 = x_3^0 = x_4^0 = 1.0$.



Figure 5. Separate surface type 1 and 2 for passive circuits: a) four nodes, $b_{n1} = b_{n2} = b_{n3} = 0$ (linear circuit); b) five nodes, $b_{n1} = \cdots = b_{n4} = 1$ (non linear circuit).

Fig. 4 (b) shows a projection of the separate surface type 1 (PSS 1) for the circuit of Fig. 3 but now using cells 1, 2 and 3, with initial values:

$$x_1^0 = x_2^0 = \dots = x_N^0 = 1.0, \qquad (7)$$

where N = 6 and $x_7^0 = x_t^0$. From Fig. 4 (b), acceleration effect is present when $x_7^0 > -0.72$ and $x_7^0 > 0.52$ or more compact $|x_7^0| > 0.72$, if the condition (7) is accomplished with $b_{n1} = b_{n2} = 0$ (linear case).

Continuing with the increment of nodes for the separate surface behavior analysis Fig. 5 shows separate surface type 1 and 2 for four nodes (a) and five node (b) passive circuits. Separate surface of Fig. 5 (a) corresponds to the circuit of Fig. 3 using cells 1, 2, 3 and 4, there are five independent variables and four dependent variables in this case. Initial conditions satisfies equation (7) with N = 8 and $x_9^0 = x_t^0$. For condition $|x_9^0| > 0.76$ acceleration effect is presented.

Finally Fig. 5 (b) shows separate surface for a non linear passive circuit, with six independent, five dependent variables and four non linear parameters y_{n1}, \dots, y_{n4} , which values satisfies equation (7) with N = 10 and $x_{11}^0 = x_t^0$. Separate surface type 2 appears when $x_6^0 = 0.63$ and $x_6^0 = -0.75$, the area enclosed by corresponding design trajectories is the prohibited region for the acceleration effect of this circuit.

3.2. Active circuits separate surface

Active nonlinear circuits of the transistor amplifiers with some transistors have been analyzed. The Ebers-Moll static model of the transistor has been used [15] to analyze all of these circuits.

3.2.1. Example 3

An active circuit of three nodes and its equivalent circuit are shown in Fig. 6. In this case we have three independent variables y_1, y_2, y_3 as admittance (K=3) and three dependent variables V_1, V_2, V_3 as nodal voltages (M=3). The state parameter vector X includes six components: $x_1^2 = y_1$, $x_2^2 = y_2$, $x_3^2 = y_3$, $x_4 = V_1$, $x_5 = V_2$, $x_6 = V_3$. The initial values of independent variables are set 1, $x_1^0 = x_2^0 = x_3^0 = 1.0$.

The variation of the initial value of the dependent variable (x_6^0) generates the MTDS family curves (Fig. 7). On the other hand, variables x_4 , x_5 are used to set up initial conditions for the transistor union voltages, as





Figure 6. One transistor amplifier:a) three nodes active circuit;b) equivalent circuit using an Ebers-Moll model.

(b)

follows:

$$V_{BEi} = x_4^0 - x_5^0 = 0.3V \tag{8}$$

$$V_{CBi} = x_4^0 - x_6^0 = -0.1V \tag{9}$$

These initial conditions are important for the numerical stability since SPICE model of Bipolar Junction Transistor (BJT) [15] has I-V exponential terms and great values of the union voltages in combination with Newton-Raphson algorithm, drives up into unstable design region [16].

The simple objective function that is used to reach the design requirements is given as:

$$C(X) = (x_6 - k_v) + (V_{BE} - \mathbf{r}_1)^2 + (V_{BC} - \mathbf{r}_2)^2 \qquad (10)$$



Figure 7. MTDS family curves and projections of separate surfaces type 1 and 2 for one transistor amplifier.

where the design condition is selected by $k_v = 6.79V$,

and terms $\mathbf{r}_1, \mathbf{r}_2$ are the final desired values for transistor's unions. The corresponding MTDS family curves and separate surfaces type 1 and 2 of design process for the circuit of Fig. 6, are shown in Fig. 7 Separate surface type 1 is defined when $x_6^0 = 8.7$ and $x_6^0 = 0.1$, while separate surface type 2 is defined when $x_6^0 = 8.7$ and $x_6^0 = 2.0$, in both cases if conditions (8) and (9) are satisfied. In consequence the acceleration effect is present for this example, when $x_6^0 < 2.0 \lor x_6^0 > 8.7$, again if the conditions (8) and (9) are satisfied.

This analysis made for one transistor circuit can be repeated for the circuits with more transistors, finding in all analyzed circuits the separate surfaces and therefore the acceleration effect of the design process.

A circuit that consists of three transistor cells is shown in Fig. 8. It is interesting to compare the design trajectories for one, two and three transistor cell circuits.

Fig. 9 corresponds to the trajectory graphs of the MTDS for three above mentioned types of the transistor amplifier. Fig. 9 (a), (b) shows the behavior of the trajectory projections in the plane $x_3 - x_6$. Fig. 9 (a) corresponds to the initial coordinate values $x_i^0 = 1.0$, and Fig. 9 (b) to the values $x_i^0 = 2.0$ for i=1,2,3. The separate lines 1 and 2 (the projections of the corresponding separate hyper surfaces) have a very strong configuration for $x_i^0 = 1.0$, that explain the presence or the absence of the acceleration effect. On the contrary, the separate hyper surface projections disappear in the plane $x_3 - x_6$ for the initial values $x_i^0 = 2.0$ (Fig. 9 (b)). It means that the acceleration effect is observed always, for any value of the coordinate x_6 because all the trajectories include the



Figure 8. Circuit topology for three-cell transistor amplifier.

possibility to jump to the final point.

It is very interesting that the circuit complication brings to the further expansion of the acceleration effect region. We can see this property from Fig. 9 (c), (d) that correspond to the two-cell transistor amplifiers. There is a significant reduction of the region of the acceleration effect absence for two cell amplifier, Fig. 9 (c). The projections of the separate hyper surface (separate lines 1 and 2) in the plane x_5 - x_{10} have the same behavior and very narrow region of the acceleration effect absence for x_i^0 =2.0, *i*=1,2,3,4,5. The acceleration effect always exists for x_i^0 =3.0 as we can see in Fig. 9 (d). The separate hyper surface disappear completely for three cell transistor amplifier (Fig. 9 (e), (f)) and we can realize acceleration effect practically for all start points and for all trajectories.

4. CONCLUSIONS

The initial point selection gives the design acceleration effect with a great probability. The trajectory analysis of various design strategies shows that the conception of the separate line or the separate hyper surface in general case is very helpful to understand and define the necessary and sufficient conditions for the design process acceleration effect existence. The separate hyper surface defines the start points and the trajectories that can produce the acceleration effect and can be used for the optimal design trajectory construction. The selection of the initial points outside of the separate hyper surface is the necessary and sufficient conditions for the acceleration effect existence.

The separate hyper surface has the complex structure in general case. However, the situation is simplified for the active nonlinear circuits because a disappearance of the separate hyper surface for more complicated circuits. It means that the acceleration effect can be realized always for the complex active circuits. This effect reduces the total computer time additionally and serves as the basis for the optimal or quasi-optimal design algorithm construction.



Figure 9. Family of the curves that correspond to the modified traditional design strategy and separate lines for: (a), (b) one-cell; (c), (d) two-cell; and (e), (f) three-cell transistor amplifier.

5. ACKNOWLEDGMENT

This work was supported by the Mexican National Council of Science and Technology CONACYT, under project SEP-2004-C01-46510.

6. REFERENCES

[1] J. R. Bunch, and D. J. Rose, (Eds), *Sparse Matrix Computations*, Acad. Press, N.Y., 1976.

[2] O. Osterby, and Z. Zlatev, *Direct Methods for Sparse Matrices*, Springer-Verlag, N.Y., 1983.

[3] A. George, "On Block Elimination for Sparse Linear Systems", *SIAM J. Numer. Anal.* Vol. 11, No.3, pp. 585-603, 1984.

[4] F. F. Wu, "Solution of Large-Scale Networks by Tearing", *IEEE Trans. Circuits Syst.*, Vol. CAS-23, No. 12, pp. 706-713, 1976.

[5] A. Sangiovanni-Vincentelli, L. K. Chen, and L. O. Chua, "An Efficient Cluster Algorithm for Tearing Large-Scale Networks", *IEEE Trans. Circuits Syst.*, Vol. CAS-24, No. 12, pp. 709-717, 1977.

[6] N. Rabat, A.E. Ruehli, G.W. Mahoney, and J.J. Coleman, "A Survey of Macromodeling", *Proc. of the IEEE Int. Symp. Circuits Systems*, pp. 139-143, April 1985.

[7] I.S. Kashirsky, and Y.K. Trokhimenko, *The Generalized Optimization of Electronic Circuits*, Tekhnika, Kiev, 1979.

[8] V. Rizzoli, A. Costanzo, and C. Cecchetti, "Numerical Optimization of Broadband Nonlinear Microwave Circuits", *IEEE MTT-S Int. Symp.*, Vol. 1, pp. 335-338, 1990.

[9] E.S. Ochotta, R.A.Rutenbar, and L.R. Carley, "Synthesis of High-Performance Analog Circuits in ASTRX/OBLX", *IEEE Trans. on CAD*, Vol.15, No. 3, pp. 273-294, 1996.

[10] A.M. Zemliak, "Analog System Design Problem Formulation by Optimum Control Theory", *IEICE Trans. on Fundament.*, Vol. E84-A, No. 8, pp. 2029-2041, 2001.

[11] A. Zemliak, "Novel Approach to the Time-Optimal System Design Methodology", *WSEAS Trans. on Systems*, Vol. 1, No. 2, pp. 177-184, 2002.

[12] E.S. Ochotta, L.R. Carley, R.A.Rutenbar, "Analog Circuit Synthesis for Large, Realistic Cells: Designing a Pipelined A/D Converter with ASTRX/OBLX", *Custom Itegrated Circuits Conf.*, Vol.15, No. 4, pp. 1-4, May 1994.

[13] A. Zemliak, "Super-Acceleration Effect of System Design Process", *Proc.* 7th. *Intl. Conf. On Mixed Design of Integrated Circuits and Systems – MIXEDES'00*, Gdynia Poland, pp. 203-208, July 2000.

[14] A. M. Zemliak, "Acceleration Effect of System Design Process", *IEICE Trans. on Fundam.*, vol. E85-A, No. 7, pp. 1751-1759, 2002.

[15] G. Massobrio, P. Antognetti, *Semiconductor Device Modeling with SPICE*, Mc. Graw-Hill, Inc., 1993.

[16] M. Bhattacharya, P. Mazumder, "Augmentation of SPICE for Simulation of Circuits Containing Resonant Tunneling Diodes", *IEEE Trans. on CAD*, Vol. 20, Jan. 2001.