PRELIMINARIES ON LOW-POWER ANALOG-TO-DIGITAL CONVERSION FOR SYSTEM-ON-CHIP DESIGN: SIGMA-DELTA MODULATORS WITH A SINGLE AMPLIFIER AND A NOVEL 14-TRANSISTOR 1-BIT FULL ADDER

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ABSTRACT

Two approaches for low-power analog-to-digital (A/D) conversion for biomedical-oriented System-on-Chip (SoC) design are addressed in this paper. The first approach introduces the use of a single amplifier to realize switched-capacitor-based 1-bit low-pass A/D sigma-delta modulators, thus reducing the power consumption of the modulator compared to the traditional counterpart (approx. 50% and 25% in 2nd- and 3rd-order modulation, respectively). Here, the single amplifier is time-shared to perform sampling and integration operations concurrently. The second approach introduces a novel small-area low-power 1-bit CMOS-based full adder cell to be used in the digital signal processing part of the SoC, which includes the digital filters of the sigma-delta A/D converters. The novel full adder comprises only 14 transistors. Compared to the standard 28-transistor full adder found in the standard library cell of the 0.35 µm 3.30 V CMOS technology used in this work, it consumes 45% less power and occupies 47% less area.

1. INTRODUCTION

The demand of high-performance low-power microelectronic-based circuits for biomedical applications grows continuously in order to boost the development of innovative medical devices and medical technologies, which are actually indispensable for delivering high-quality healthcare [1]. In contrast to that proposed in [2], a biomedical-oriented system-on-chip (SoC) that encapsulates a number of subsystems (e.g. analog front-ends, A/D converters, dedicated digital filters, a digital signal processor and related memory) for the acquisition, digitization and processing of biosignals (e.g. electrocardiographic signals) will help develop less power consuming (i.e. battery powered), more compact, and more versatile systems. Consequently, low-power design and small-area circuits are mandatory for the design of such SoC.

Sigma-delta (ΣΔ) modulators, which are widely used in high-resolution A/D conversion because of their robustness with respect to the inaccuracies of the analog components, are chosen to be employed in the SoC. In [3] the traditional architecture of a 1-bit low-pass N^{th}-order single-loop ΣΔ-modulator is explained. This architecture corresponds to a chain of N SC-integrators with distributed feedback; thereby, the power consumed by the active components, i.e. amplifiers, increases when N also does. In order to reduce the power consumption, an alternative structure which makes use of a single amplifier to conceive the N^{th}-order ΣΔ-modulator for $N > 1$ is presented. The alternative structure performs the sampling and integration operations concurrently within the sampling period T_s, while the number of integrations defining the modulation order is attained by time-sharing the single amplifier [4].

Since addition operations are extensively used in digital signal processing (e.g., in the decimation filters succeeding the A/D ΣΔ-modulators), a low-power small-area 14-transistor 1-bit adder cell with rail-to-rail output swing is presented. The cell is designed and laid out in a 0.35 µm 3.30 V CMOS technology [5] and is meant to replace the 28-transistor 1-bit standard CMOS adder [6] provided by the technology supplier. Several few-transistor-count adder cells have been proposed in the literature [7]-[8], but have the disadvantage of demanding more than 14 transistors, which negatively impact the area of the cell, or of not producing full swing output signals, which worsens the noise margin and the driving capability of the cell, and makes subsequent buffering stages dissipate considerable amounts of power.

This paper is organized as follows: Section 2 addresses the working principle of the single amplifier ΣΔ-modulators and points out their advantages; Section 3 presents simulation results and discusses a possible circuit implementation of the new modulators; Section 4 introduces the principle of operation of the proposed 1-bit adder and provides simulation results; conclusions are given in Section 5.

2. WORKING PRINCIPLE OF THE SINGLE AMPLIFIER ΣΔ-MODULATOR

Consider the SC-circuit depicted in Fig. 1. During $\phi_1 = 1$ the signal at input V_1 is sampled into C_{s1}, and the charge in C_{s2} is accumulated into C_{f2}. When ϕ_2 is active, the charge contained in C_{s1} is dumped into C_{f1}, and at the same time the output voltage is sampled into C_{s2}. The processing of input V_2 is similar to that of input V_1, except that it is sampled twice both during ϕ_1 and ϕ_2. Note that sampling and integration take place concurrently.

Assuming ideal switches and amplifiers, it can be demonstrated following the analysis procedure of [9] that, if the inputs and output of the SC-circuit are taken when ϕ_1 is active, the transfer functions $V_{out}(z)/V_1(z)$ and $V_{out}(z)/V_2(z)$ are

$$\frac{V_{out}(z)}{V_1(z)} = H_1(z) = \frac{a_1 a_2 z^{-1}}{\left(1 - z^{-1}\right)^2} \tag{1}$$

$$\frac{V_{out}(z)}{V_2(z)} = H_2(z) = \frac{a_2 b_1 z^{-1}}{\left(1 - z^{-1}\right)^2} + \frac{b_2 z^{-1}}{1 - z^{-1}} \quad , \tag{2}$$

with $a_1 = C_{s1}/C_{f1}$, $a_2 = C_{s2}/C_{f2}$, $b_1 = C'_{s1}/C_{f1}$ and $b_2 = C'_{s2}/C_{f2}$. By time-sharing the amplifier, the circuit realizes a double-integration on V_1 as well as a single- and double-integration on V_2 within T_s, which are precisely the operations a traditional 2nd-order ΣΔ-modulator performs on its input and feedback signals, respectively. Ultimately, the single-amplifier SC-circuit of Fig. 1 is employed to derive the 1-bit 2nd-order ΣΔ-modulator shown in Fig. 2, with a simpler clocking scheme as well as fewer switches than the one-opamp 2nd-order modulator reported in [10]. The modulator's signal transfer function *STF(z)* and noise transfer function *NTF(z)* are given by

$$STF(z) = \frac{a_1 a_2 z^{-1}}{1 + (a_2 b_1 + b_2 - 2) z^{-1} + (1 - b_2) z^{-2}} \quad , \tag{3}$$

$$NTF(z) = \frac{\left(1 - z^{-1}\right)^{-2}}{1 + (a_2 b_1 + b_2 - 2) z^{-1} + (1 - b_2) z^{-2}}$$

where the quantiser is modeled as an additive white-noise source.

In Fig. 3, the proposed concept is extended to a 1-bit single-amplifier 3rd-order ΣΔ-modulator, wherein the amplifier has a time of $T_s/3$ to execute each integration. The corresponding *STF(z)* and *NTF(z)* can be demonstrated to be

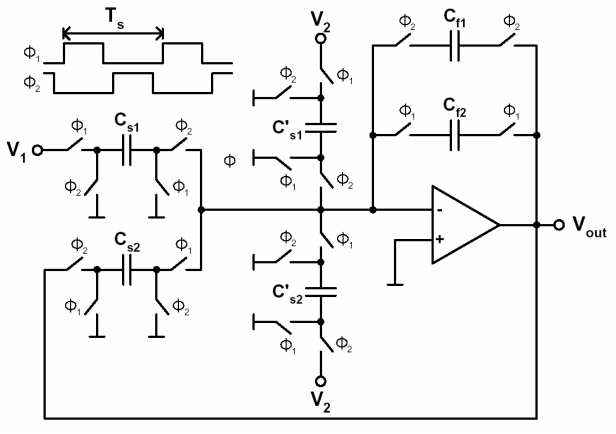


Fig. 1. Concurrent sampling and integration SC-circuit.

$$STF(z) = \frac{a_1 a_2 a_3 z^{-1}}{1 + \alpha z^{-1} + \beta z^{-2} + \delta z^{-3}} \quad , \tag{4a}$$

$$NTF(z) = \frac{\left(1 - z^{-1}\right)^{-3}}{1 + \alpha z^{-1} + \beta z^{-2} + \delta z^{-3}}$$

with

$$\begin{aligned} \alpha &= a_2 a_3 b_1 + a_3 b_2 + b_3 - 3 \\ \beta &= 3 - 2b_3 - a_3 b_2 \\ \delta &= b_3 - 1 \end{aligned} \quad , \tag{4b}$$

and $a_1 = C_{s1}/C_{f1}$, $a_2 = C_{s2}/C_{f2}$, $a_3 = C_{s3}/C_{f3}$, $b_1 = C'_{s1}/C_{f1}$, $b_2 = C'_{s2}/C_{f2}$, $b_3 = C'_{s3}/C_{f3}$.

However, a higher modulation order N demands the amplifier to be faster since each integration has to be completed within a time T_s/N, thus imposing a limit to the feasibility of the approach from the power consumption standpoint.

2.1. Power considerations

Assuming that an operational-transconductance amplifier (OTA) is utilised as amplifier and that its settling time is linear and non-slew-rate limited when working as an SC-integrator, the reasoning considered in [11] will be followed in order to gain insights about the power consumption in terms of bias currents. Thus, for the amplifier in the traditional Nth-order modulator's SC-integrator (denoted OTA1), the relationship between speed and power consumption is determined by

$$GBWP_1 = \frac{1}{C_1} \cdot \sqrt{2K \cdot \frac{W_1}{L_1} \cdot I_{DS1}} \quad , \tag{5}$$

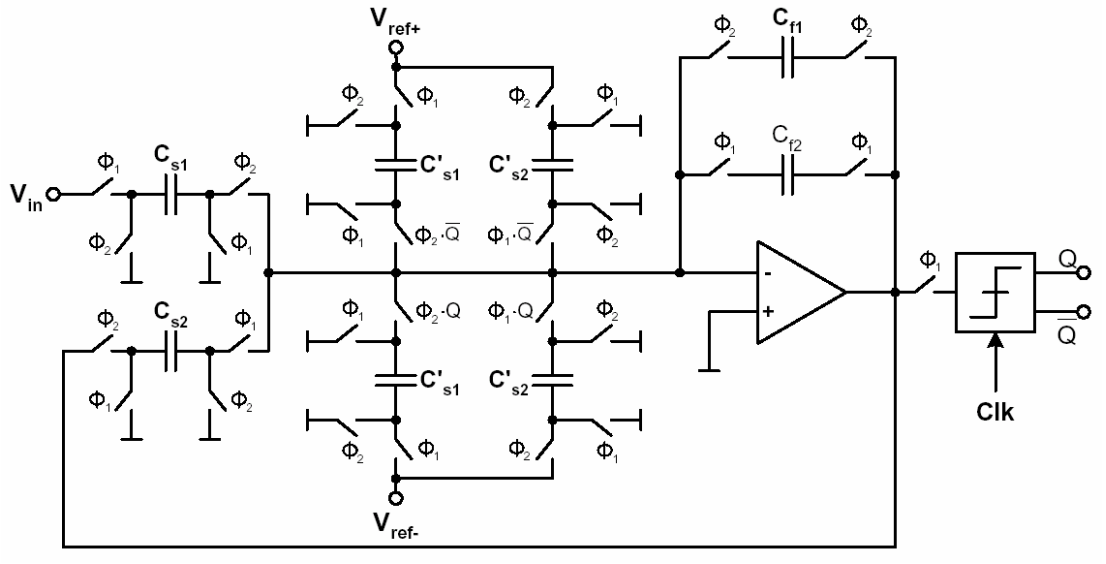


Fig. 2. Circuit-level representation of the 1-bit 2nd-order ΣΔ-modulator.

where $GBWP_1$ is the OTA's gain-bandwidth product, C_1 is the total equivalent loading capacitance in its integrator functionality, K, W_1 and L_1 are the input stage transistor's transconductance parameter, width and length, respectively, and I_{DS1} the bias current through those transistors. Consequently, the traditional N^{th}-order modulator, where each SC-integrator has a time of $T_s/2$ to perform the integration, consumes a power directly proportional to $N \cdot I_{DS1}$, assuming that the amplifiers within the last N-1 SC-integrators are not scaled.

On the other hand, in a single-amplifier N^{th}-order ΣΔ-modulator there is a time of T_s/N for it to compute one integration. In this case, the amplifier (denoted OTA2) needs to be $N/2$ times faster than OTA1, i.e.

$$GBWP_2 = \frac{N}{2} \cdot GBWP_1 = \frac{1}{C_1} \cdot \sqrt{2K \frac{W_1}{L_1} \left(\frac{N^2}{4} \cdot I_{DS1} \right)} \; ; (6)$$

therefore, OTA2 consumes a power directly proportional to $(N^2/4) \cdot I_{DS1}$ for transistor geometries and loading conditions similar to OTA1. As a consequence, in a 2nd-order and a 3rd-order modulator, 50% and 25% of the power is saved, respectively, by the single-amplifier approach, while in a 4th-order modulator no power is saved anymore.

3. SIMULATION RESULTS: 2ND-AND 3RD-ORDER SINGLE-AMPLIFIER ΣΔ-MODULATORS

The SC-circuits of Figs. 2 and 3 have been simulated with SWITCAP2 in order to corroborate the functionality and the performance of the 1-bit single-amplifier ΣΔ-modulation concept. The coefficients of the modulators are $a_1 = b_1 = 0.25$, $a_2 = b_2 = 0.125$, $a_3 = b_3 = 0.50$, which both guarantee that the outputs of the OTA remain bounded within the reference voltages and make the 3rd-order single-amplifier modulator be conditionally stable according to the root locus criteria [12].

The test signal is a 0.50 V, 100 Hz sinus signal. The sampling frequency f_s is 100 kHz and the reference voltages are ±1.65 V. The number of output samples acquired is 100000. Figure 4(a) plots the power spectrum density (PSD) of the systems of Figs. 2 and 3. The 2nd-order and 3rd-order modulators achieve 69.2 dB and 87.6 dB signal-to-noise ratio (SNR), respectively, for an oversampling ratio of 128. These values have been also confirmed through Matlab/Simulink simulations. The SNR versus input-power characteristic of the proposed modulators has been computed with Matlab/Simulink and is to be seen in Fig. 4(b). Dynamic ranges (DR) of 78.6 dB (~12.8 bits resolution) in the 2nd-order case and of 94.4 dB (~15.4 bits resolution) in the 3rd-order case are obtained. Note that only quantization noise is taken into account in these simulations. Therefore, the DR will be less in an actual circuit realization.

An exhaustive analysis of the circuit-level design of low-power single-amplifier modulators is currently being carried out. Although the effects of OTA's non-idealities, such as incomplete settling time, slew-rate, finite amplifier gain and amplifier noise, as well as the noise aliasing issues in SC-circuits have been widely studied in order to quantify their impact on the traditional modulator's performance [13], these effects need to be mapped to the proposed SC-structures. Other effects such as the on-resistance of the

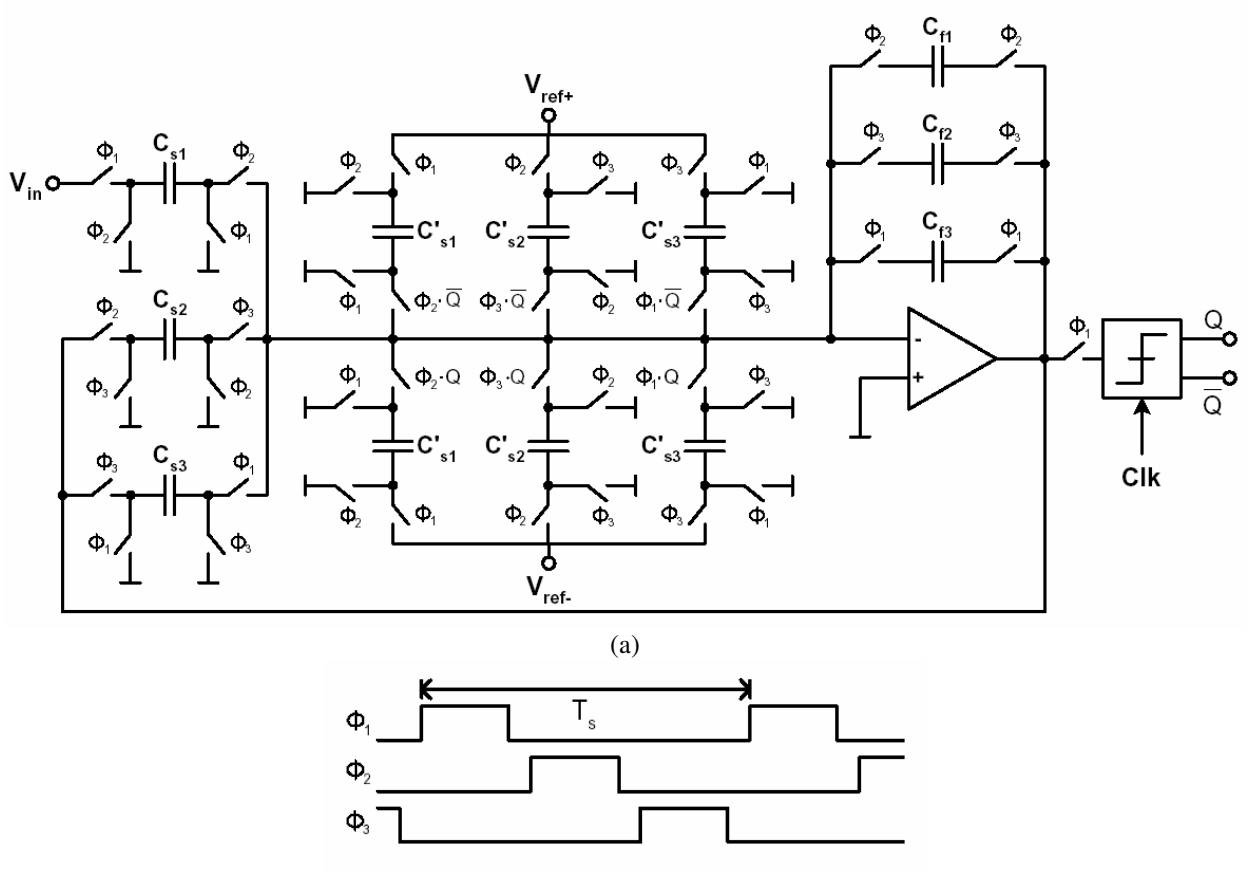


Fig. 3. Circuit-level representation of the 1-bit 3rd-order ΣΔ-modulator: (a) schematic, (b) clocking scheme.

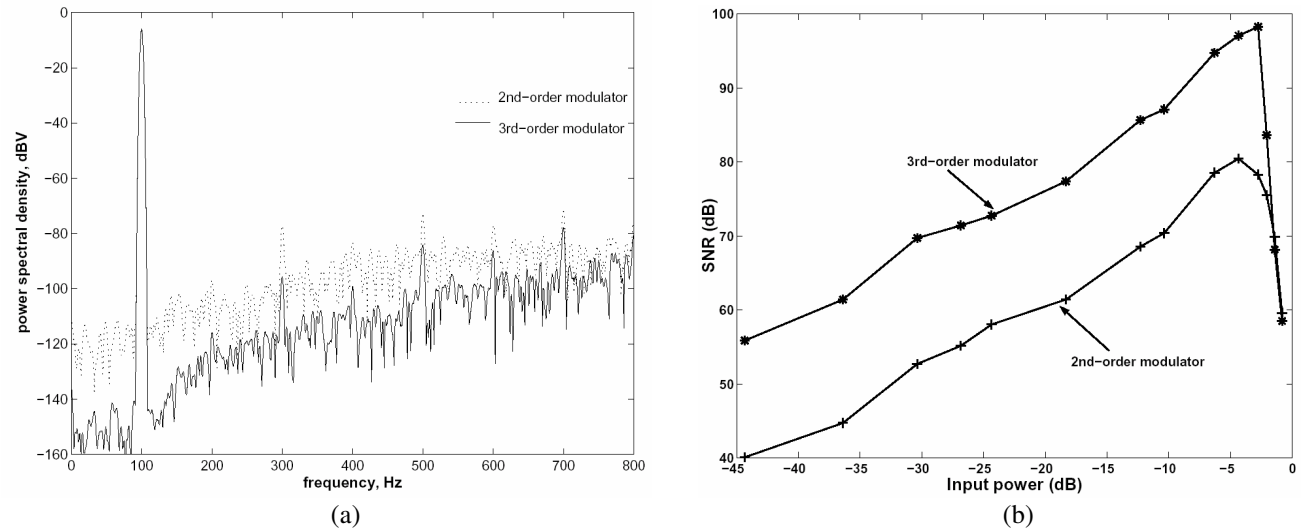


Fig. 4. (a) Power spectrum of the single-amplifier modulators, and (b) SNR vs. input power characteristic.

sampling and feedback switches can be made unimportant [14]. Charge-injection induced errors on the feedback capacitances can degrade the system's performance and need to be minimized [15]. Once this analysis is completed and the feasibility of the single-amplifier approach for 1-bit ΣΔ-modulation is restated, a methodology for its optimum design will be developed. In addition to that, the suitability of multi-bit single-amplifier modulators has to be also

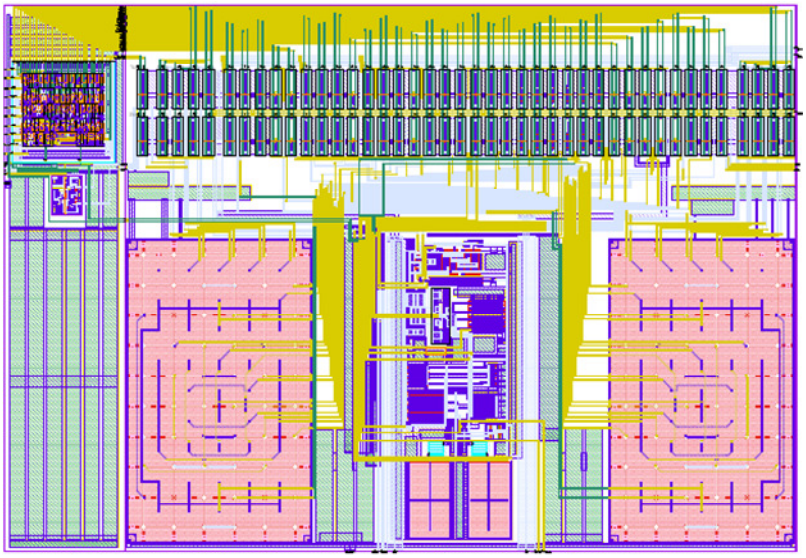


Fig. 5. Layout view of the 1-bit 3rd-order single-amplifier ΣΔ-modulator.

investigated.

The 2nd- and 3rd-order single-amplifier modulators have been already prototyped on silicon [16], using a 0.35 µm CMOS technology. For the circuit implementation, a programmable 2-stage class A/AB fully-differential opamp [17], a regenerative comparator [13], NMOS/CMOS switches and poly-poly capacitors were utilized. These circuits will serve as test vehicles for the verification of the theoretical analysis mentioned in the last paragraph. Figure 5 shows the layout view of the 3rd-order ΣΔ-modulator. Measurement results on these modulators will be reported in future work.

4. THE NOVEL 14-TRANSISTOR FULL ADDER CELL: PRINCIPLE OF OPERATION

It is well known that the power consumed in a digital CMOS circuit depends on the supply voltage, the clock frequency, the internal node switching activities, the internal node capacitances, the internal short-circuit currents, and the number of internal nodes [18]. Thus, if a 1-bit adder cell is to be designed efficiently, assuming that the power supply and the clock frequency are fixed parameters and that the switching activity is controlled at the architectural level, the circuit implementation has to have as few transistors (preferably with minimum feature size), circuit nodes and direct paths between the power supply and ground as possible. The former indication aims at decreasing the amount of capacitive loads (i.e., at decreasing the dynamic power component), whereas the latter addresses the short-circuit currents (i.e., the short-circuit term). Note that these measures also help decreasing the physical size of the cell. To avoid increasing the short-circuit power in subsequent buffering stages, the adder cell must deliver full swing outputs.

To address the indications cited above, the approach of [19] is followed. By expressing the sum S and carry-out C_{out} output bits as

$$\begin{aligned} S &= H \oplus C_{in} = H \cdot \overline{C_{in}} + \overline{H} \cdot C_{in} \\ C_{out} &= A \cdot \overline{H} + C_{in} \cdot H \ , \end{aligned} \tag{7}$$

where

$$H = A \oplus B \ , \tag{8}$$

the adder can be divided into three modules, as seen in Fig. 6. On the one hand, *module-2* is efficiently devised using the transmission function implementation of an XOR gate shown in Fig. 7(a), which allows the module to have minimum transistor count, to provide a full output swing, and to consume the lowest average power. On the other hand, *module-3* is efficiently implemented as a pass-gate 2-to-1 multiplexer with H acting as the "select" input. Hence, *module-3* is able to provide rail-to-rail outputs. Its schematic is depicted in Fig. 7(b).

Concerning the conception of the *module-1*, it is desirable that H and its complement feature a full swing to enhance the signal integrity characteristics of these signals and to assure a rail-to-rail swing at the S output. This can be done if *module-1* is realized as suggested in [8] and shown in Fig. 7(c). The cross-coupled PMOS transistors perform a pseudo-XOR operation, since they disable

themselves for *A*=*B*="1". Besides, they are not able to fully pass a logic "0". Similarly, the cross-coupled NMOS transistors are not able to fully pass a logic "1", performing a pseudo-XNOR operation, since they disable themselves for *A*=*B*="0". It is precisely the function of the additional NMOS and PMOS transistors, which are connected in a positive-feedback configuration, to circumvent these problems. When *A*=*B*="1" occurs, the node *H* is driven to a full logic "0" and its complement to full logic "1" through the action of the cross-coupled NMOS transistors and the positive-feedback. Likewise, for the combination *A*=*B*="0", the cross-couple PMOS transistors initially passes a signal close to ground at node *H*, and the positive-feedback action produces a full logic "0" and a full logic "1" at node *H* and its complement, respectively.

Hence, the proposed low-power small-area 1-bit adder cell is made up of the modules presented in Fig. 7, and can be considered as the optimum ensemble out of the low-power (LP) full adder found in [7] and the N-Cell1 adder found in [8]. The schematic view of the proposed cell is drawn in Fig. 8. Many other 1-bit adder cells reported elsewhere [20] prove to have more transistors and consume more power at the reference switching frequency of 50 MHz. Novel low-power adder cells claim to use 14 [21], 12 [22] or even 10 transistors [23]; however, the output voltage levels of the cells are known to be severely degraded [20] and they do not take into account that this makes the short-circuit currents of subsequent buffering stages greatly increase. For this reason, these novel cells are deemed to be inefficient in terms of power consumption compared to the proposed adder cell.

4.1. Simulation environment and results

The simulation environment emulates a very-likely operating scenario, wherein inverters (buffers) drive the cell's inputs whereas the *S* and C_{out} outputs are loaded with an inverter, each of which drives a lumped capacitance. The simulations are carried out with Cadence Spectre.

Functional verification is done by applying to the inputs *A*, *B*, C_{in}, a Matlab-generated 3-bit pattern with all possible 64 transitions (since each input exhibits 4 possible transitions, namely, "0" → "0", "0" → "1", "1" → "1", and "1" → "0"). This also permits to look for the worst-case timing. Functional verification has been run on the LP, N-Cell1 and the proposed adder cell for a 0.35 μm 3.30 V CMOS technology, assuming a 50 MHz switching frequency and using feature sizes close to minimum (transistor aspect ratio smaller than 1.43). A snapshot of the waveforms generated by the N-Cell1 and the proposed adders is appreciated in Fig. 9. As expected, the results showed that all cells satisfied (1). Note that the *S* output signal of the N-Cell1 adder is not rail-to-rail though.

Estimations of the power dissipation are conducted by applying a Matlab-generated random sequence of 1000 bits to each input, where the "0" and "1" are generated with

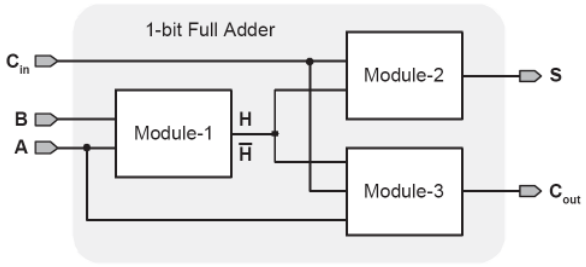
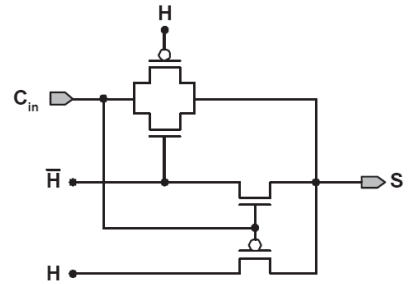
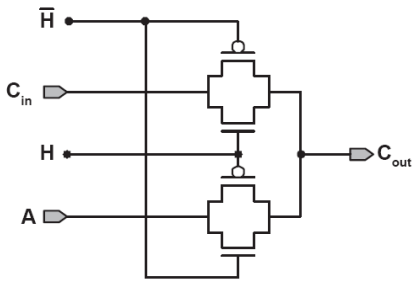


Fig. 6. Modularization of the 1-bit full adder.



(a)



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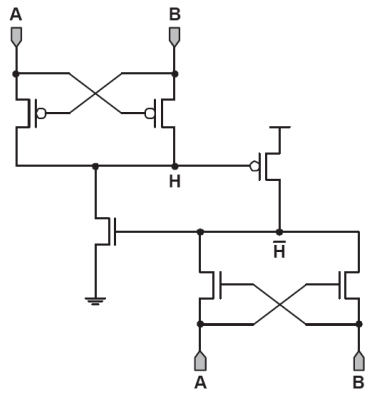


(c)

Fig. 7. Realization of (a) *module-2*, (b) *module-3*, and (c) *module-1*.

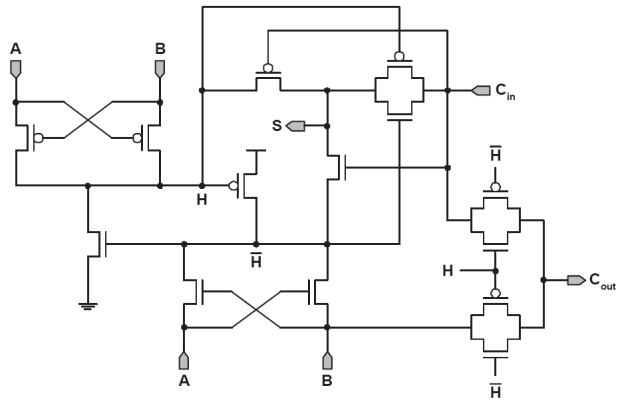


Fig. 8. Transistor-level implementation of the proposed 1-bit adder.

equal probability [21]. The switching frequency of the pattern as well as its transition times are set in Matlab. The average power of the cells is then computed with Spectre. Power estimations have been computed on the pre-layout versions of the LP, N-Cell1 and the proposed structures, as well as on the 28-transistor standard CMOS 1-bit adder found in the 0.35 μm technology digital library, assuming a switching frequency of 50 MHz, and a lumped capacitance of 100 fF. The results are contained in Table 1, showing that the N-Cell1 and the proposed adder are good candidates for small-area design; but, it is the proposed cell which achieves full swing outputs, consumes the lowest power and makes the output buffers it drives dissipate far less power than those driven by the N-Cell1 adder. Therefore, it is the proposed cell that satisfies the small-area and low-power requirements demanded in SoC-based applications.

Functional verification and power estimations have been also carried out after backannotating post-layout parasitic information on both the proposed cell and the standard CMOS cell. Post-layout simulation data are shown in Table 2 and the actual cell layout in Fig. 10(a). The proposed cell is 47% smaller and dissipates about 45% less power. Nevertheless, it is slower than the standard adder by a factor of 2. This, however, does no represent a problem since many biomedical signals are low-bandwidth.

4.2. Design flow of the customized digital cell

A Cadence-based design flow is followed after proving the feasibility of the proposed cell in order to include it in the synthesis and floorplanning-placement-routing (FPR) flows of major digital circuits. The main steps are:

- Schematic entry with Virtuoso Schematic Composer.

Table 1. Summary of pre-layout simulation results

Cell	N°. of transistors	Full swing outputs	Power drawn by (in μW @ 50 MHz)	
			Cell	Output buffers
Standard	28	Yes	12.48	30.43
LP	16	Yes	8.27	31.35
N-Cell1	14	No	3.90	57.22
Proposed	14	Yes	3.84	32.06

Table 2. Post-layout simulation results

Cell	Area	Power (@ 50 MHz)	Delay (ns)
Standard	13.0 μm × 21.0 μm	13.93 μW	0.55
Proposed	13.0 μm × 11.2 μm	7.63 μW	1.20

- Layout completion with Virtuoso Layout-XL Editor.
- Generation of the *lib*- and Timing Library Format (TLF) files containing timing characterization data. The Cadence Open Command Environment for Analysis (OCEAN) tool is well recommended for this.
- Creation of the abstract view with Cadence Abstract Generator. This view, seen in Fig. 10(b), is created based on the layout view and is used to generate the Library Exchange Format (LEF) file containing the cell's physical data.

The resulting *lib*-file is used by Synopsys tools to perform logical synthesis and/or static timing analysis of the gate-level synthesized circuits. Subsequently, the LEF file, which contains the basic physical information to instruct the FPR tool about the cell dimensions, pins location and metal obstructions; and the TLF file, are used to run the FPR flow in Cadence Silicon Ensemble.

5. CONCLUSIONS

The realization of 1-bit 2^{nd}- and 3^{rd}-order single-amplifier single-loop A/D ΣΔ-modulators and a 14-transistor low-power small-area 1-bit full adder cell has been addressed. It was shown that these approaches represent an attractive solution for low-power biomedical-oriented SoC design. The impact of non-idealities on the performance of first approach will be reported in future works.

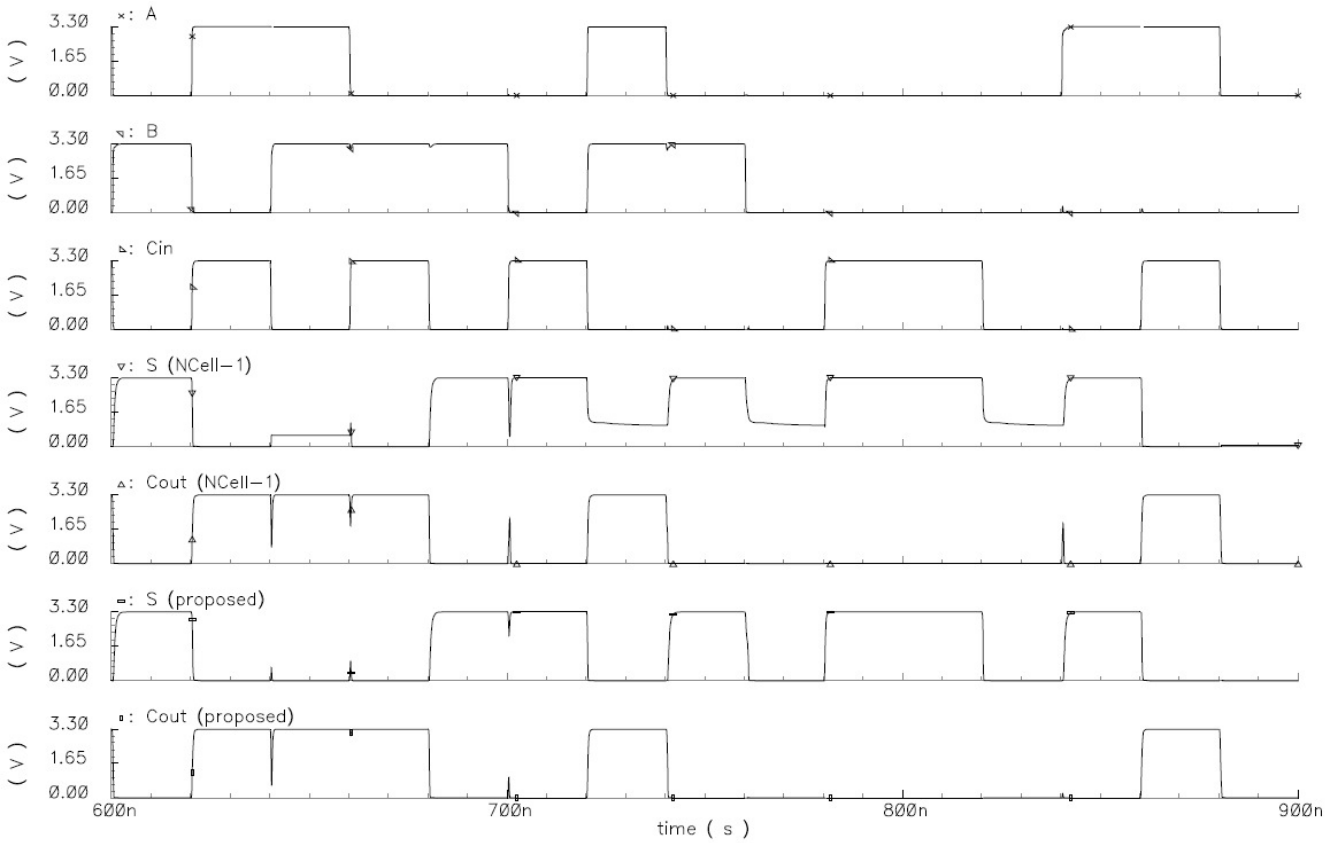
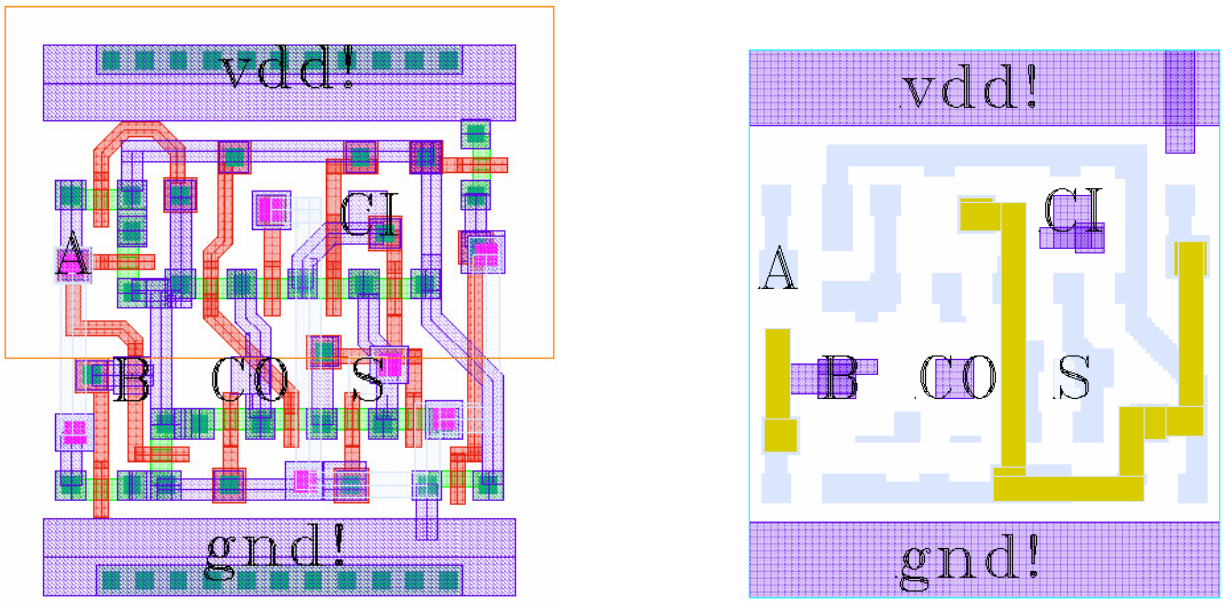


Fig. 9. Snapshot of the waveforms generated by the NCell-1and the proposed adder. The waveforms of the LP adder (not shown) simply follow those of the proposed adder.



(a) (b)

Fig. 10. (a) Layout and (b) abstract views of the proposed adder cell (height = 13.0 µm, width = 11.2 µm).

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