DESIGN OF A 12-BIT 44MSPS PIPELINE ADC FOR MULTI-STANDARD DIGITAL RADIO IN 0.13um CMOS TECHNOLOGY

F. Medeiro[1,2], A. Charlet[1], C. Utrera[1], J.A. Segovia[1], A. Sánchez-Franco[1], M. Guerra[1], R. Castro[2], J. Ruiz-Amaya[2], M. Delgado-Restituto[2], and A. Rodríguez-Vázquez[1,2]

[1]AnaFocus [2]Instituto de Microelectrónica de Sevilla

medeiro@imse.cnm.es

ABSTRACT

This paper presents the design of a low-cost 12-bit Analog-to-Digital Converter (ADC) for digital radio applications in a 0.13um CMOS technology. It employs a 10-stage pipelined architecture preceded by a sample-and-hold (S/H) block that multiplexes two single-ended or differential input signals. The ADC delivers 12-bit data up to 44MSPS, which enables its use in other high frequency applications, such us video-rate data acquisition, high-speed data transmission, and wireline communications. The complete cell, including on-chip voltage and current reference generation, occupies 1mm^2 and consumes 200mW at full speed when supplied with 3.3V.

1. INTRODUCTION

Digital radio is receiving an ever increasing attention from radio broadcasters and users. Apart from the increased number of channels and interference-free reception quality, digital radio enables multimedia data reception by end users, including text, pictures, and even video.

To the already existing DAB (Digital Audio Broadcasting) [1], a new standard called DRM (Digital Radio Mondiale) [2] is being incorporated. Unlike digital systems that require a new frequency allocation, the DRM signal is designed to fit in with the existing AM broadcast band plan, based on signals of 9 kHz or 10kHz bandwidth. It has modes requiring as little as 4.5kHz or 5kHz bandwidth, plus modes that can take advantage of wider bandwidths, up to 20kHz.

New software/hardware developments are being carried at the industry side to give support to these standards. From the hardware point of view, like in other application scenarios (video, wireless communications, etc.) multi-standard capability is added to a set of already challenging requirements, such as high-resolution, low power consumption (essential for mobile equipments) and compactness. The latter has prompted maximal integration, which ends up with the necessity of high-performance analog functions implemented in digital-oriented deep-submicron CMOS processes.

In this paper we present the design of a 12-bit pipeline ADC for digital radio in 0.13um CMOS. In order to cope with present and forthcoming standards, the ADC can operate up to 44MSPS, including specific modes for DAB and DRM. In DAB applications, the ADC operates in undersampling mode, i.e. converting a narrow-band signal centered at a frequency much higher than the sampling rate. In DRM mode, classical Nyquist-rate conversion is allowed, but it requires only half of the maximum output rate. In order to optimize the ADC consumption with respect to the power budget in each operating mode, a programmable bias current mechanism is implemented.

The rest of this paper is organized at follows: Section 2 presents the ADC architecture. The main sub-blocks, the content of a pipeline stage and the S/H circuit, are described in Sections 3 and 4, respectively. Section 4 is devoted to circuit design aspects. Also in this section, the design of the building blocks is illustrated. Finally, Section 5 summarizes available results.

2. ADC ARCHITECTURE

Figure 1 shows the converter architecture. It consists of a 10-stage pipelined ADC using redundant multi-bit quantization and correction logic. In order to improve linearity [3], the first stage uses 3bit quantization whereas the rest use 2bits. The last stage is just a 2bit flash ADC. This architecture establishes a good trade-off between circuit complexity and performance, with reduced power consumption [4].

While clk is high, the analog input is being sampled differentially at the input sample-and-hold capacitors. The sampled input is held at the falling edge of clk. While clk is low, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage.

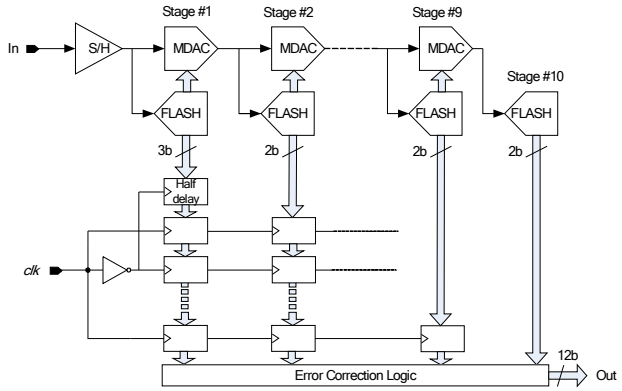

Figure 1 – 10-stage pipeline ADC architecture

When clk goes back high, the first stage produces its residue, which is acquired by the second stage. At the same time, the input S/H goes back to acquiring a new analog input sample. When clk goes low again, the second stage produces its residue, which is acquired by the third stage. An identical process is repeated for the remaining stages, resulting in a 9th stage residue that is sent to the 10th stage ADC for final evaluation. With this timing the ADC exhibits a latency of 6 clock cycles (including the S/H).

Results from all the stages are digitally synchronized such that the results can be properly combined in the correction logic before being sent to the output buffers.

3. PIPELINE STAGES

Each pipelined stage contains a quantizer (flash ADC), a reconstruction digital-to-analog converter (DAC) and an inter-stage residue amplifier. The two latter functions are actually integrated in a single block, the so-called multiplying DAC (MDAC). In operation, the ADC quantizes the input to the stage and the quantized value, re-converted to the analog domain by the DAC, is subtracted from the input to produce a residue. The residue is amplified and output by the residue amplifier.

Figure 2 shows the schematic of the MDAC in an *N*-bit implemented using switched-capacitor (SC) circuitry. During the sampling phase, the input signal is stored in 2^{N-1} identical capacitors, while the OTA is reset. During the residue-amplification amplification, one of these capacitors is placed in a feedback configuration around the OTA, whereas the remaining ones sample either the positive or the negative reference voltages, depending on the output of the flash quantizer in the stage. In this converter, 4 unitary capacitors are used in the first stage (7-level DAC) and only 2 in stages 2 to 9, which require a 3-level DAC. Due to the fact that only 3 levels need to be discerned in the second and following stages, instead of the $2^2 = 4$ levels present in a regular 2-bit ADC justifies the appellative "1.5-bit per stage" normally accompanying such topologies [5]. For the same reason, the first stage is not 3bit but 2.8bit

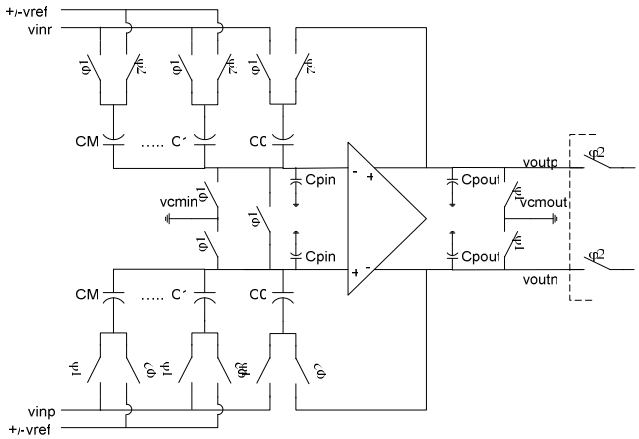

Figure 2 – MDAC schematic

These comparison levels are determined in the in-stage quantizer. Since the required resolution is low, a flash ADC is used for such purpose. Figure 3 shows the schematic of the 7-level flash ADC in the first stage. It is composed of 6 fully-differential comparators that receive the thresholds from a resistor ladder. After generation of the thermometric code, it is encoded to control the MDAC switches. Also, a redundant 3-bit code is passed to the digital part. The use of edge-triggered D flip-flops prevents from metastability of the preceding comparators.

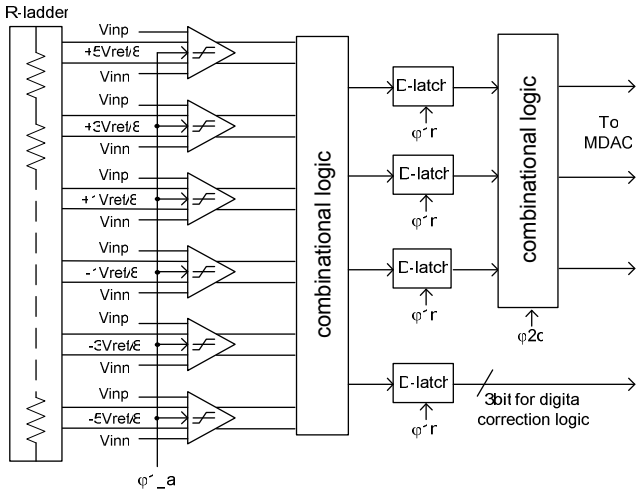

Figure 3 – 7-level flash ADC

The quantizers in the remaining stages use a similar topology but only two comparators are required in the 3-level flash ADC. The comparators, based on regenerative latches, are strobbed slightly before the end of the sampling phase, while the input signal is being stored at the MDAC sampling capacitors. With this timing the decision made is available to control the MDAC switching at the beginning of residue-amplification phase.

Figure 4 shows the residue characteristics of each pipeline stage.

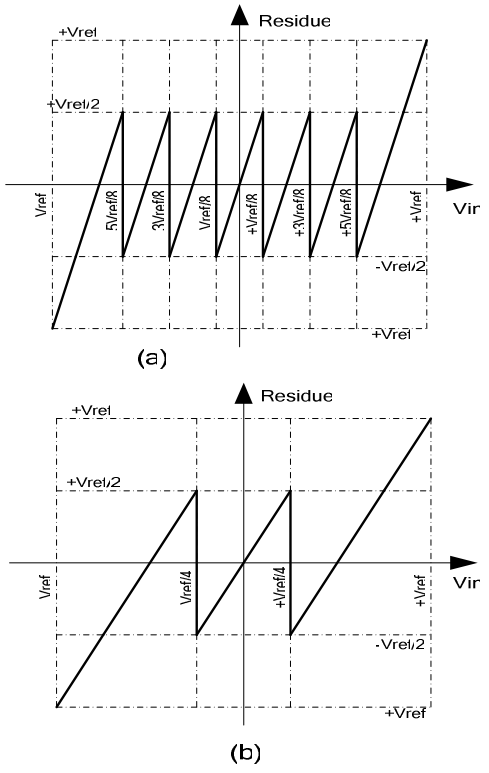

Figure 4 – Residue of the (a) 3-bit stage, (b) 2-bit stages

3. S/H AMPLIFIER

Since the intended applications require accommodating both single-ended and differential input signals, an SC amplifier is used as S/H circuit. Its simplified schematic is shown in Figure 5. Two differential or single-ended signals can be multiplexed at the sample-and-hold input: *vinp*1-*vinn*1 and *vinp*2-*vinn*2. The second input (*vinp*2-*vinn*2), not shown, is accommodated by duplicating the whole input branches shown. This guaranties good isolation from input to input at very high frequencies.

The sample-and-hold circuit consists of a switched-capacitor amplifier operated with two non-overlapped clock phases: during the sampling phase (φsa high), input voltage is stored at capacitors Cin, while the amplifier (not used in this phase) is forced to its quiescent input and output voltages. During the holding phase (φho high), the charge stored at C_{in} is forced to the feedback capacitors C_{fb}, resulting in an output voltage equal to $vout = (C_{in} / C_{fb})\ vin$.

For differential inputs, the switches to the left of capacitors C_{fb} sample the input common-mode voltage, while the right plates of these capacitors (V_A and V_B) are connected to the output common-mode voltage. However, for single-ended inputs, referred to ground, the latter are connected to *vrefn* (upper branch) and *vrefp* (lower branch), so that 0 volt single-ended input is translated into a negative differential voltage equal to *vrefn*-*vrefp*. By properly scaling the capacitors, the biggest single-ended input of interest is translated into *vrefp*-*vrefn*. This operation does not affect the OTA common-mode input and output voltages, which are dynamically kept at proper values.

The input sample-and-hold is designed to accommodate two different signal full-scale ranges, namely 1.25Vpp and 2.5Vpp. This is achieved by switching the gain of the switched-capacitor amplifier between two values, by adapting the value of the sampling capacitor C_{in}, while keeping fixed the feedback one. This is the reason why two identical input branches are shown in Figure 5. When low gain is selected only one of the branches is actually switched.

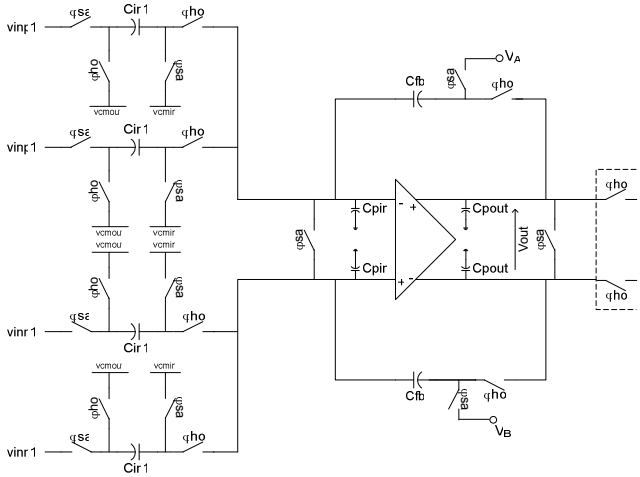

Figure 5 – Simplified schematic of the S/H amplifier

4. CIRCUIT DESIGN CONSIDERATIONS

The signal-to-(noise+distortion) ratio (*SNDR* or *SINAD*) of an ADC is approximately given by the following relationship,

$$SINAD(dB) = 10\log_{10}\left[\frac{V_{ref}^{\ 2}}{2(P_Q + P_N + P_{HD})}\right]$$

where V_{ref} stands for the reference voltage, ultimately defined by the supply voltage, and P_Q, P_N, and P_{HD} are the in-band powers of quantization error, circuit noise, and distortion, respectively.

Scaling down the supply voltage by a factor α directly maps into a proportional decrease of the reference voltage that can be used and, hence, imposes a reduction of the signal power by a factor α^2. Also, quantization noise power P_Q scales down in the same proportion. However, circuit noise P_N and distortion P_{HD} do not scale automatically, but keep essentially constant. The latter may be even bigger due to non-linearities of the building blocks (OTAs,

switches, etc.), which are more evident in a low-voltage context.

Thus, to keep a given *SINAD*, both circuit noise and harmonic distortion must be lowered by design in the same factor α^2. Both aspects are carefully considered next.

4.1. Circuit noise

Like in most discrete-time data circuits, noise generated by the OTAs and switch on resistances are sampled by the switched capacitors at the clock frequency. In order to achieve good enough settling within the available time-slot (half a clock period), the time constant of the switch on resistance and the associated capacitor is chosen to be several times smaller than the clock period. With this, the equivalent bandwidth of the noise becomes larger than half the sampling frequency and aliasing of the sampled noise spectra takes place. This gives rise to the well-known kT/C noise contributions.

In every ADC stage, the noise generated in the MDAC switches and OTA suffers from aliasing and so does the noise that the stage receives from the previous one and from the reference voltage generator.

Fortunately, given that each MDAC has a gain higher than unity, their contributions to the overall input-equivalent noise are progressively attenuated as we go from the first to the last pipelined stage. So, while the first stage noise directly adds to the input-equivalent noise, that of the backend stages are almost negligible. This interesting feature allows scaling down the backend stages with respect to noise, thus resulting in a more efficient design.

For this purpose, detailed theoretical noise models have been used to get initial estimates of noise-related circuit parameters (such as size of unitary capacitors, switch on resistance, OTA dynamics, etc.). In addition, behavioral simulation including circuit noise models has been employed to fine-tune these figures.

As a matter of example, Figure 6 shows the fully-differential SC schematic of a MDAC. During phase phi1 (sampling), noise generated in the switch on-resistance shown is sampled at the input capacitors. In this process, since the equivalent bandwidth of this noise is higher than half the sampling frequency, the noise is undersampled and hence its power spectral density is folded back. During phase phi2 (residue generation and amplification) the noise of the switched on-resistance displayed and also that of the OTA is sampled at the following MDAC input stage and the process continues along the pipelined stages. Table 1 collects the noise contributors to the output-equivalent noise of a pipelined MDAC. The total noise power is obtained as the summation of all the contributions. Similar equations were obtained for the S/H amplifier

Table 1 – Summary of MDAC circuit noise contributors

Contributing "noisy" element	Expression for MDAC output noise power
Input switches sampled and held by MDAC capacitors at the end of the sampling phase	$P_{noise,1} = 2 * \frac{kT}{C_M + \ldots + C_1 + C_0} * G_{MDAC}^2$
Reference switches, broadband filtered by equivalent noise bandwidth of MDAC during residue amplification phase	$P_{noise,2} = 2 * 4kT * \frac{R_{on,switch\_ref}}{M} * \frac{UGBW_{RA}}{4 * G_{MDAC}} G_{MDAC}^2$
Reference generation block, broadband filtered by equivalent noise bandwidth of MDAC during residue amplification phase	$P_{noise,3} = psd_{R1\_VREF} * G_{VREF}^2 * \min(\frac{UGBW_{VREF}}{4 * G_{VREF}}, \frac{UGBW_{RA}}{4 * G_{MDAC}}) * G_{MDAC}^2$ $P_{noise,4} = psd_{R2\_VREF} * 1^2 * \min(\frac{UGBW_{VREF}}{4 * G_{VREF}}, \frac{UGBW_{RA}}{4 * G_{MDAC}}) * G_{MDAC}^2$ $P_{noise,5} = psd_{OTA\_VREF} * \frac{1}{\beta_{VREF}^2} * \min(\frac{UGBW_{VREF}}{4}, \frac{UGBW_{RA}}{4 * G_{MDAC}}) * G_{MDAC}^2$
MDAC OTA, broadband filtered by equivalent noise bandwidth of MDAC during residue amplification phase	$P_{noise,6} = psd_{OTA\_MDAC} * \frac{1}{\beta_{RA}^2} * \frac{UGBW_{RA}}{4} * 1^2$

G_{MDAC} is the gain of the MDAC during the residue amplification phase.
$R_{on,switch\_ref}$ is the on resistance of the switches connected to +/- Vref.
$UGBW_{RA}$ is the unity gain bandwidth of the MDAC OTA with feedback factor during the residue amplification phase.
psd_{R1_VREF} is the noise power spectral density of the resistor R1 of the VREF stage.
psd_{R2_VREF} is the noise power spectral density of the resistor R2 of the VREF stage.
psd_{OTA_VREF} is the noise power spectral density of the OTA of the VREF stage.
G_{VREF} is the gain of the VREF stage.
$UGBW_{VREF}$ is the unity gain bandwidth of the VREF OTA with feedback factor.
psd_{noise,OTA_MDAC} is the noise power spectral density of the OTA of the MDAC stage.
β_{VREF} is the feedback factor of the VREF stage.
β_{RA} is the feedback factor of the MDAC stage during the residue amplification phase.

It is worth noticing that low-frequency noise

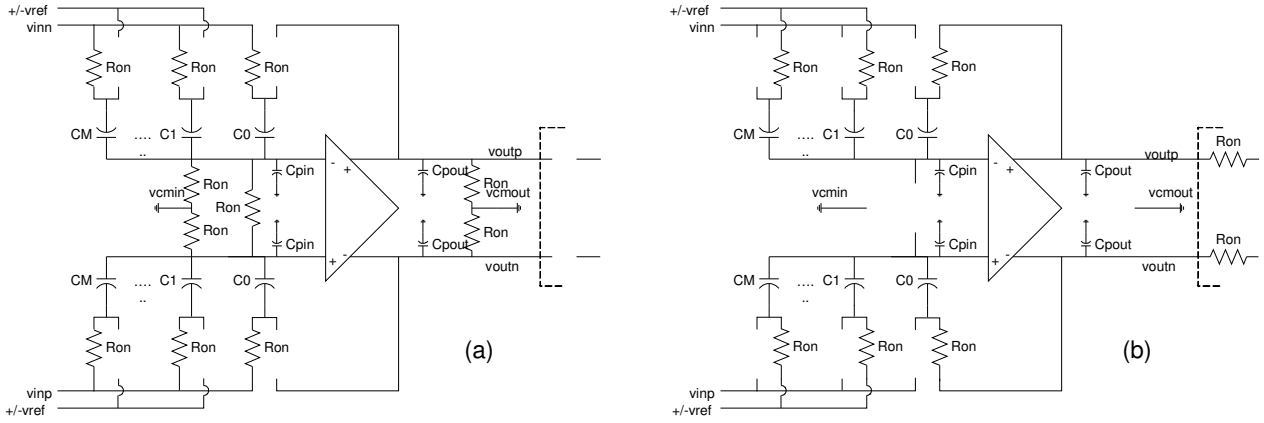

Figure 6 – MDAC configurations during (a) sampling and (b) residue amplification showing noise contributors

components (such as flicker noise generated by the OTAs) are not undersampled and hence its contribution to the overall circuit noise power is certainly negligible.

Figure 7 shows a comparative of the S/H and MDAC noise powers when referred to the ADC input. Note that the S/H and the first MDAC are the blocks contributing most to the overall noise, while the relative importance decreases in the backend stages. In fact, the value of the unitary capacitor (for noise considerations set to 0.5pF, and 0.9pF at the S/H and first MDAC, respectively), is progressively scaled down to 80fF used in the two last MDAC stages.

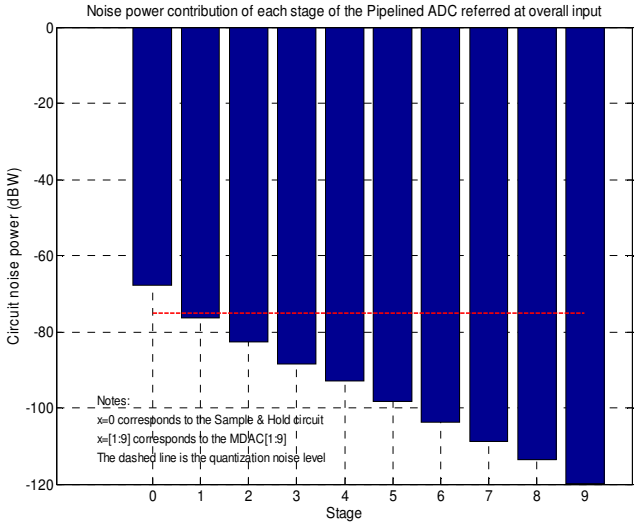

Figure 7 – Comparative of noise contributions of the S/H and ADC stages

4.2. OTAs

Apart from electronic noise, the OTAs in the S/H and MDACs may be source of non-linearity. This can be either static, due to insufficient and/or non-linear open-loop DC gain, or dynamic, associated to limited gain-bandwidth product and, mostly, slew-rate.

In practice, both static and dynamic characteristics are intimately related to the signal swing required at the OTA's output. This is because in order to get high DC gain, on the one hand MOS devices must be properly saturated, which requires a significant voltage drop, the higher the faster the dynamic requirements (i.e. the more biasing current); on the other, due to output conductance degradation, a single output device might not be sufficient for achieving high DC gain, thus requiring cascode structures and, hence, more voltage drops. Exemplified in Figure 8(a), this results in open loop DC gain that considerably varies along the signal swing (shadowed area), thus creating distortion and limiting the useful signal range.

This triple gain-speed-range trade-off can be alleviated by resorting to two-stage OTAs. These are in general more power-hungry than their single-stage counterparts but one can achieve almost rail-to-rail swing with high, constant open-loop gain; see example in Figure 8(b).

Figure 9 shows the schematic of the OTA in the S/H stage. This is the most demanding in terms of open-loop gain, noise and dynamics. As a result, a powerful topology has been selected. It consists of a pMOS-input folded-cascode first stage plus a nMOS-input differential-pair-based second stage. This topology allows us to get almost rail-to-rail output swing with a good control of the current in the second stage. The amplifier uses cascode compensation for better stability and lower power consumption. It also uses a regulated cascode current source at the differential input pair for improving common-mode rejection ratio (CMRR), especially important when the input is single-ended.

The rest of OTAs in the MDACs, use a similar topology but without regulated cascode current source because they actually work with differential signals. Also the folded-cascode input stage was replaced by telescope one. Moreover, thanks to the decreasing impact of the backend MDACs on the overall resolution, their OTAs can be progressively scaled down, thus lowering power and area.

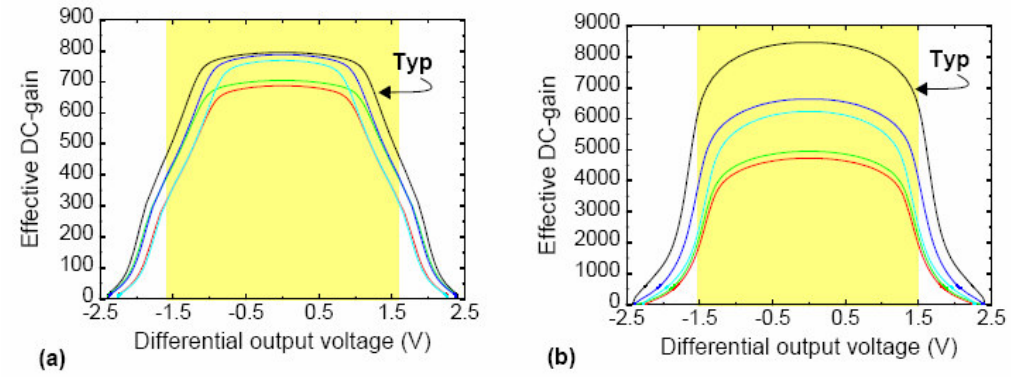

Figure 8 - Effective open-loop DC-gain for (a) folded-cascode OTA; (b) two-stage OTA

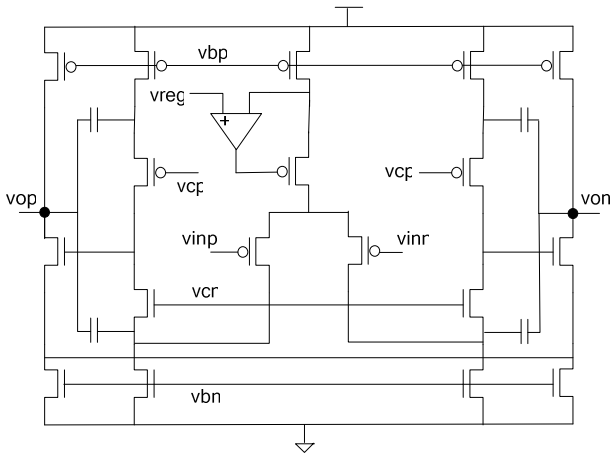

Figure 9 – Core of the fully-differential two-stage OTA used in first MDACs and S/H block

4.3. Switches

When in on state, analog switches used in SC circuits must provide small enough resistance in order to allow good settling behavior. Moreover, this on resistance should be constant along the signal range in order not to provoke dynamic distortion. That is why CMOS switches are normally used. However, both objectives are difficult to fulfill in low-voltage implementations; basically because the threshold voltages of the MOS devices do not scale down in the same proportion as the supply voltage, thus decreasing the range in which the on-resistance keeps approximately constant, see Figure 10. It may even happen that no one of the complementary MOS is conducting in a given range, i.e. a "dead" zone would appear in the signal swing for which the switch is actually off. Fortunately, this is not the case, even in worst-case conditions, for usual 0.13um CMOS processes.

If thick-oxide MOS devices (capable of operating with around 3.3V nominal supply) are available, the use of such devices in critical switches can solve the problem because the constant-resistance range is much more noticeable in these switches, see Figure 10.

If not, or wherever the on-resitance is not constant enough over process corners, temperature and supply, the Vgs voltage applied to the switching device can be boosted to make it independent of the signal being transmitted. This can be done with the circuit shown in Figure 11 [6], where the supply voltage is dynamically added to the signal voltage, so that Vgs = Vdd, no matter the input level. Moreover, the circuit is conceived to keep voltages Vgs, Vgd, and Vds of the switching device within the rate operating voltage of the technology, so that device reliability can be assured.

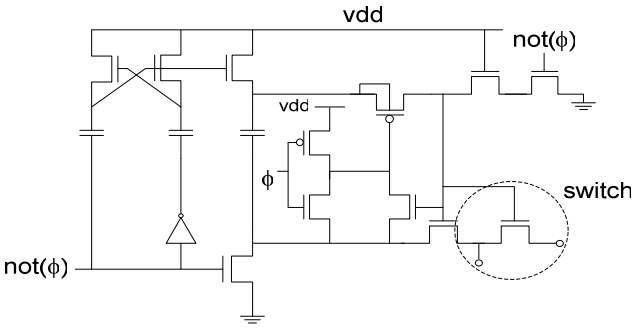

Figure 11 - Bootstrap circuit and switch

In the intended technology 3.3V thick-oxide transistors are available, and they are selected for all the analog subblocks, including the switches. However, simulations revealed the need for boosting input switches in the sample-and-hold circuit and in the first MDAC, in order to limit dynamic distortion for high-frequency input signals, especially in single-ended input mode. Also, boosting input switches reduces its overall on-resistance, thus enabling high full-power bandwidth, which is essential for undersampling applications.

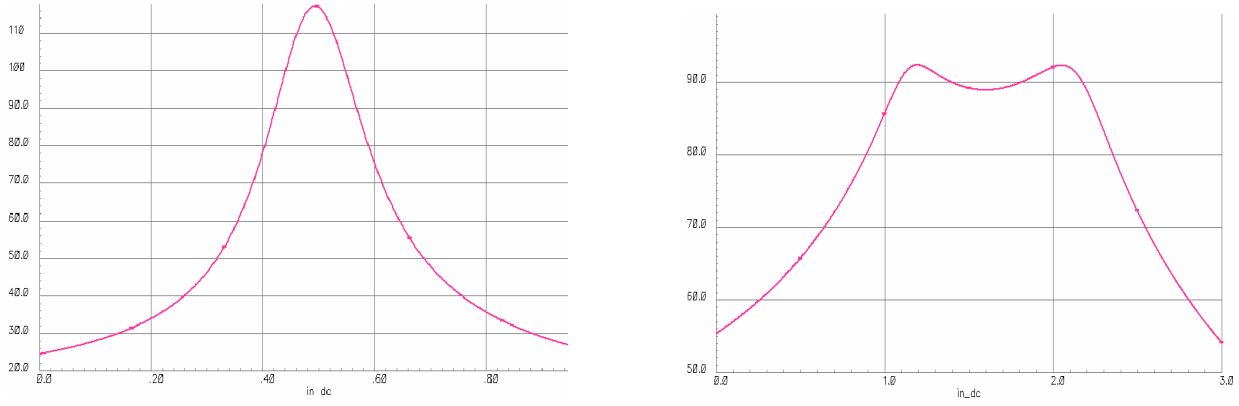

Figure 10 – On-resistance vs. voltage for 1.2V (left) switch, and 3.3V (right) switch, in the same 0.13um CMOS technology.

4.4. Flash quantizers and comparators

The correction logic usually included in pipelined ADCs renders them very insensitive to circuit imperfections in the quantizers of each stage, so that no special techniques for offset, gain, and non-linearity correction are actually required in these blocks. For this reason, the simple differential-input flash quantizer shown in Figure 3 is adopted.

The most important specification of its main building block, the comparator, is that it must solve in short enough time. For this purpose, the regenerative latch shown in Figure 12 is used. It compares the differential input with a differential reference voltage obtained by resistive division from the reference voltage (*vrefp-vrefn*).

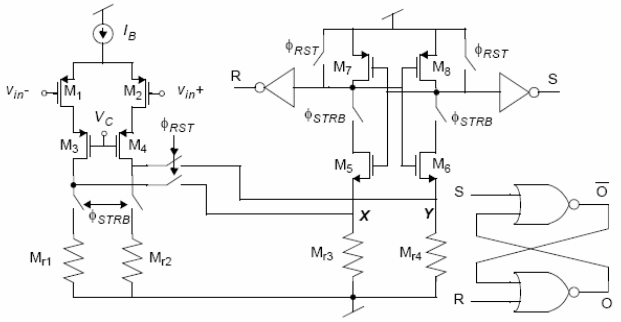

Figure 12 - Low kick-back noise comparator with regenerative latch

In this topology, resistors M_{r1} to M_{r4} are actually implemented with MOS transistors in ohmic region, with their gates connected to the supply. It uses a cascode differential input pair, which reduces kickback noise. For the same reason, the input pair is not switched off when the latch is released, but its current is derived to ground.

4.5. Reference voltage and current generation

The cell includes the on-chip reference generation circuitry shown in Figure 13. The seed for reference generation can be obtained from an on-chip bandgap voltage generator or from a dedicated external input *vrefin*. The reference input (from bandgap or external) is properly buffered before entering a resistive amplifier that generates the differential reference voltage (*vref* = *vrefp-vrefn*) around the common-mode *vcm*, obtained by resistive division from supply. The common-mode voltage is also buffered to be accessed externally.

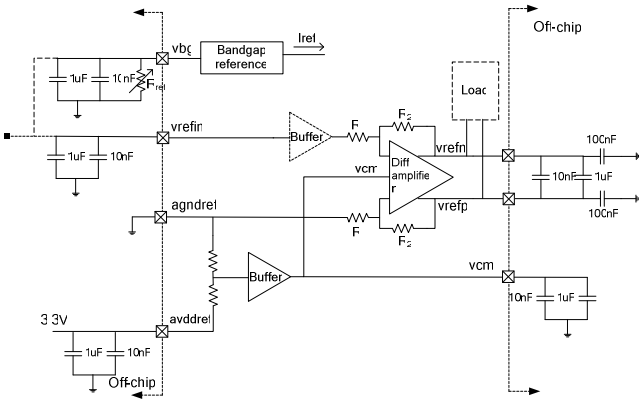

Figure 13 – On-chip reference generation circuitry

The bandgap is also employed for generating a stable reference current for biasing the OTAs. The simplified circuitry is shown in Figure 14. For better control of the refence current, a low-spreading external resistor is used. The actual bias current can be programmed to be adapted to the ADC operation mode.

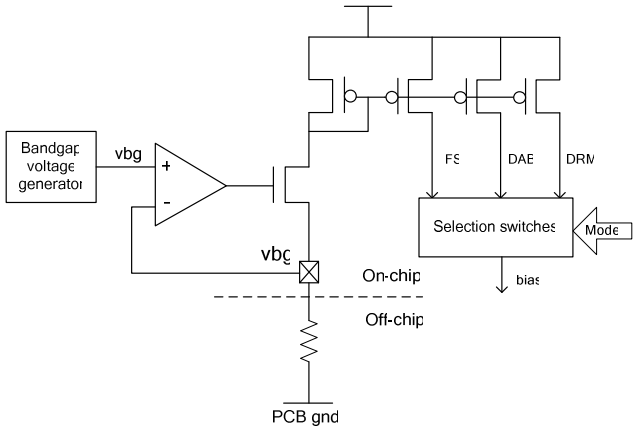

Figure 14 – Schematic for bias current generation

5. ILLUSTRATIVE RESULTS

The complete ADC has been exhaustively simulated both at behavioral level (using SIMSIDES [7]) and full-electrical level (using SPECTRE). These simulations included process, temperature (-40, 125degC), supply (3.3±10%) and clock duty-cycle (±20%) variations, as well as device mismatch, especially capacitors. Capacitors used are metal-insulator-metal capacitors (MiM) with 1fF/um^2 and good matching properties (1%/sqrt(um^2) area low).

Figure 15 shows typical output spectra obtained from behavioral simulations at 44MSPS for 7.5MHz and 22MHz full-scale sinewaves (edge of the Nyquist band). Note that in-band error power is dominated by noise (quantization + circuit noise).

Figure 16 shows the 256-point FFT of output sampled at 44MSPS when the S/H-ADC is simulated at device level (using SPECTRE) with a full-scale, 2.58MHz sinewave. Total Harmonic Distortion (THD), dominated by the presence of a 3rd-order harmonic, is -75dB – low enough for the required effective resolution (min. 10bit ENOB).

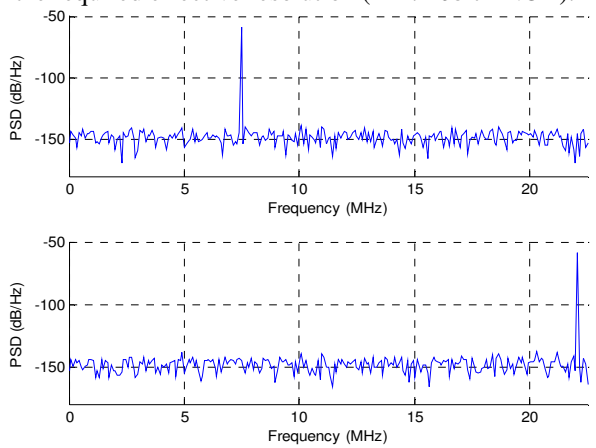

Figure 15 – Simulated output spectra for full-scale 7.5MHz (top) and 22MHz (bottom) input sinewave

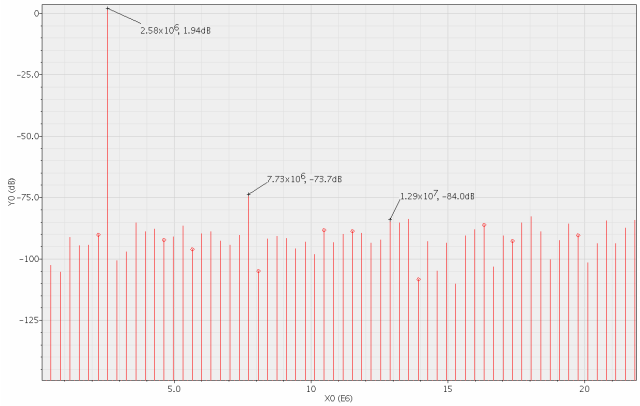

Figure 16 – ADC output spectra for a full-scale input at 2.58MHz (from full-electrical simulation)

The simulations above do not include capacitor mismatch. When it is included, non-linearity dominates the error power so that a SINAD distribution like that in Figure 17 is obtained. The worst-case value is almost 63dB, which correspond to 10.2bit ENOB.

In the same conditions the differential (DNL) and integral (INL) non-linearity curves shown in Figure 18 are obtained. INL is bounded by +1.38/-1.75LSB (referred to 12bit).

Table 2 summarizes the main performance parameters.

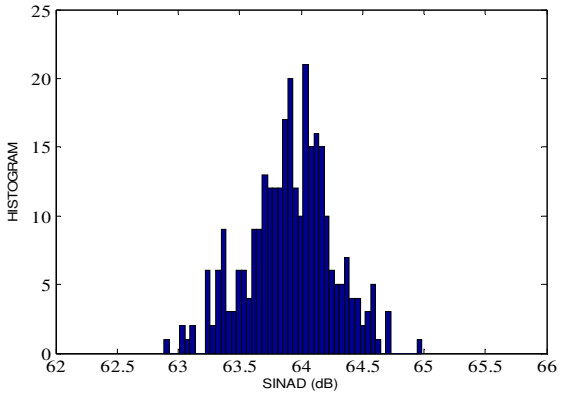

Figure 17 – Histogram of simulated SINAD including capacitor mismatch (from behavioral simulations, for input signals at the edge of the Nyquist band)

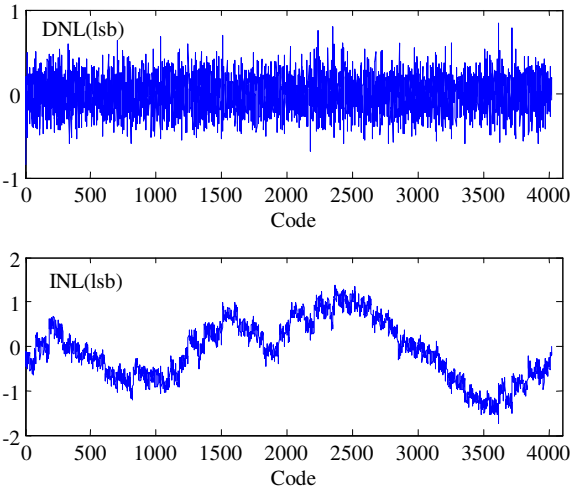

Figure 18 – DNL and INL obtained from behavioral simulations

Table 2 – Main ADC performance parameters

Resolution	12bit
Conversion rate	44MSPS
Input range	1.25 or 2.5Vpp
ENOB at Niquist	10bit (w.c.), 11bit (typ.)
DNL (12bit)	<±0.8LSB
INL (12bit)	<±1.8LSB
Power cons. (3.3V)	200mW @ 44MSPS 100mW @ 24.6MSPS (DRM) 40mW @ 8.2MSPS (DAB)
Active area	1mm^2

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