

# INTRODUCING DIGITAL IC DESIGN AND TEST TO UNDERGRADUATE STUDENTS

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## ABSTRACT

This paper presents the ITM's efforts to introduce to undergraduate students IC design in two basic ways: digital CMOS design and non-destructive test and electrical characterization. In the *Instituto Tecnológico de Merida* (ITM) where there were not previous work on research and teaching IC technology, some efforts have to be made in such a way that our students start to gain IC knowledge. Strategies to reach this goal are presented as well as a short description of the ITM's academic plan, which includes improve laboratory experience. From such plan, an IC formed by a Digital PLL frequency synthesizer was fabricated in a 1.5 $\mu\text{m}$ , 5-V CMOS technology. This IC is the first one designed in any academic institution of the so-called Maya-region.

## 1. INTRODUCTION

Microelectronics is one of the most important industries in the world. Almost every consumer product contains one or more electronic system. From cellular phones and digital video to modern automobiles, all of these contain electronically controlled and/or programmable parts. Electronics products even help to improve life quality of people with physical limitations, where applications like hearing aids and pacemakers are just some examples. Considering these facts, it is not a surprise to know about the tremendous growth of the electronics industry since the past decade. Today, the trend is developing whole Systems on a Chip (SoC), that is: integrate all the electronic system's functions, including digital and analog circuits, on a single silicon die. Every day new products go out to the market offering less power consumption, reduced size, altogether with additional functions and capabilities. By one side, it is important to consider that CMOS and BiCMOS technologies have played an important role in this development of the integrated applications. Currently,

modern CMOS technologies offer possibilities to integrate such circuits as RF transmitters and receivers with all kind of digital functions. On the other hand, the most important universities in the world are investing a mayor part of their efforts and resources in preparing and educating students in all these trends, so they can incorporate them to their future jobs with the skills required by the semiconductor and microelectronics industries. Unfortunately, many universities cannot afford the high costs associated with the infrastructure required to provide this kind of education. Software for IC design and laboratory facilities are out of budget for these institutions. These kinds of problems are more notorious in countries with poor and/or medium technological development. For instance, in Mexico, integrated circuit design education is provided by CINVESTAV and INAOE<sup>1</sup>, through graduate degrees on microelectronics and related topics. Undergraduate studies, in contrast, oriented to this research area are offered in very few institutions, where generally these studies are at simulation level.

This paper describes the efforts made in the ITM to relate undergraduate students toward CMOS digital integrated circuit design and test concepts. Design and fabrication of an IC that covers topics of an undergraduate course will be presented as follows. In section 2, a discussion about the options for IC design teaching is analyzed. An IC Digital Phase Locked-Loop (DPLL) oriented for frequency synthesizer test in a PLL design course is presented in section 3. Simulation and measured results are also given in the same section. At the end of the paper the conclusions of this academic experience are given.

## 2. STRATEGIES FOR IC DESIGN AT ITM

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<sup>1</sup> Both graduate programs and research areas can be found in [www.inaoep.mx](http://www.inaoep.mx)

Application Specific Integrated Circuit (ASIC) design can be incorporated to undergraduate courses by teaching how to take advantage of digital concepts by introducing programmable logic devices like FPGA's [1], [2]. Next, high integration of logic functions can be accomplished with low cost development boards oriented for education, i.e. facilities offered by Digilent [3]. For instance, the Xilinx University Program allows to academic institutions the opportunity to access software development tools as ISE-Webpack and Modelsim simulators [4] in a free way. ASIC design along with VHDL or another language can be taught in Digital Design courses. The disadvantage of such an approach is that students miss the opportunity to learn other aspects of integrated circuit design. Such teaching strategy does not allow students face mixed signal design problems, which means that the project development would be based on digital systems only (see Figure 1). Currently, it is well known there is a trend in industry to incorporate not only digital but also RF and IF sections into a single silicon die.

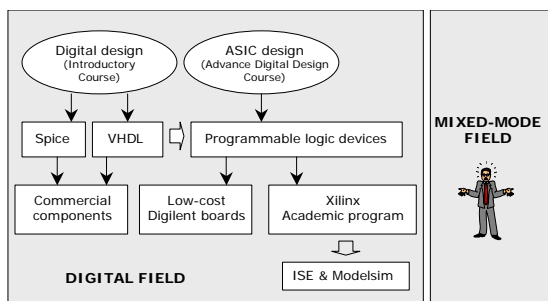


Figure 1. The ITM's strategy to teach IC design based on CMOS technologies: The beginning step.

CMOS digital and analog integrated circuit design can be taught to students using open source or free software. Currently there are free IC layout software tools that can be used to undergraduate teaching, Magic [5], Electric [6] and LASI [7] are some examples. Our choice was LASI due its Windows compatibility. On the other hand, circuit simulation can be done with free software like WinSPICE [7]. Finally, to close the design cycle IC projects are fabricated through MOSIS.

Since the undergraduate curriculum of the Electrical and Electronics Department at ITM does not include any course related with IC design (digital or analog), we have defined the following strategy. Firstly, students with the desire to enroll in learning IC design could develop a project through a well-defined Senior Design Project course held in the eight semester. Then, they would have the option to do –during his/her final academic activity- a thesis project. According this strategy the first projects were based on simple circuits and systems because their results and design procedures will be used in the next

academic year's introductory courses, i.e. before the semester 8th. Here the idea is enhance these courses with a real IC application, where newest IC students can learn and understand the main limitations of a CMOS implementation, about spice simulation as well as optimize the design of our first IC, and so on up to have a suitable teaching CMOS cells library.

### 3. INTEGRATED CIRCUIT DEFINITION

Since high percentage of modern systems for communication applications are based on digital blocks, the definition of our first IC was a digital design. The selected blocks are described in the following.

#### 3.1. IC building blocks

As shown in Figure 2, a PLL based frequency synthesizer was designed. This system consists of a Phase Frequency Detector (PFD), Loop Filter (off chip), Voltage Controlled Oscillator (VCO) and a fixed frequency divider. Each basic block is also oriented for doing laboratory work and project design in an undergraduate PLL design course. Being oriented to teaching CMOS IC design and test; the chip contains the whole DPLL as well as every circuit block for using as a stand-alone circuit. Students can, as a consequence, test, analyze and characterize each block for behavioral simulation and design of the off chip loop filter.

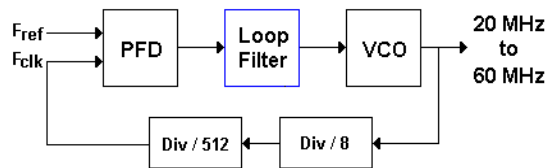


Figure 2. DPLL based frequency synthesizer.

#### 3.2. Circuit design and layout

The PFD was implemented using a conventional 3-state detector [8], as shown in Figure 3. In this design the bias voltage was  $V_{DD} = 5V$ , and for simulation purposes a capacitive load was taken into account,  $C_L = 15pF$ . In practice  $C_L$  represents the total load due IC-package and PCB parasitics. The layout,  $255 \times 51 \mu m^2$ , was designed in such a way that the height of the PDF corresponds to each basic cell's height. By designing each cell with such a characteristic, it is possible their use as standard cells in future designs.

Figure 4 shows the Voltage Controlled Oscillator (VCO) that is a current-starved ring oscillator type [8]. The VCO simulation showed a center frequency of approximately 40 MHz for  $V_{in} = 2.5V$ . Here a capacitive load of 15pF was assumed.

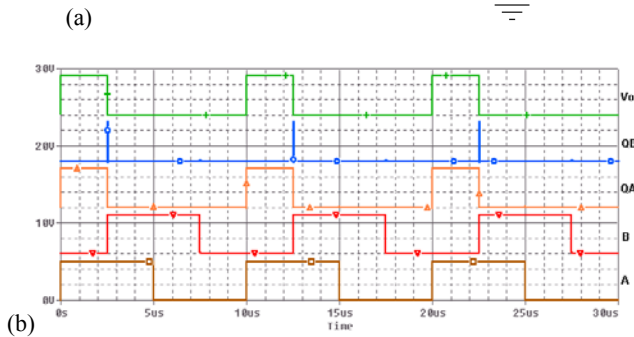
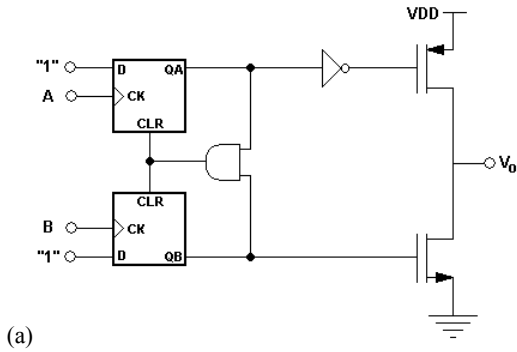


Figure 3. Schematic of the conventional PFD circuit (a); spice simulation results (b). Here “1”= $V_{DD}$ .

As we have seen from Figure 2 the PLL uses two frequency dividers: a divide-by-8 and a divide-by-512 circuits. The first one is used for dividing the high frequency signal that comes from the VCO’s output, while the last one is required to use the DPLL as a frequency synthesizer.

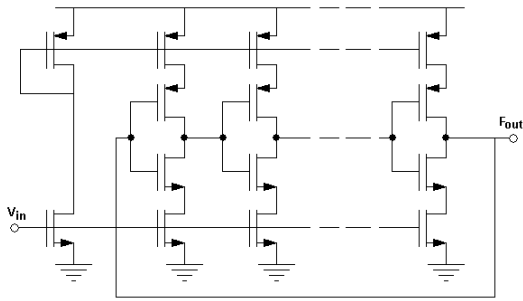


Figure 4. Current starved VCO circuit. In this design the series connected stages correspond to an odd number.

The frequency dividers have been designed from D Flip-Flops as shown in Figure 5. Here the D Flip-Flops were designed to be a compact basic cell of our library. As the divide-by-8 circuit has input frequencies in the order of MHz, it was implemented using dynamic D Flip-Flops as depicted in Figure 6. It is known that dynamic logic circuits allow high frequency operation respect static circuits [8]. From Spice simulation a maximum frequency  $f=200$  MHz was obtained.

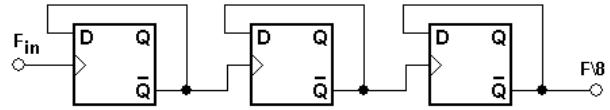


Figure 5. Divide-by-8 divider schematic.

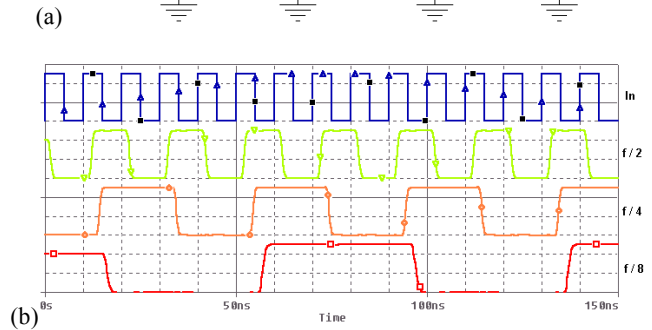
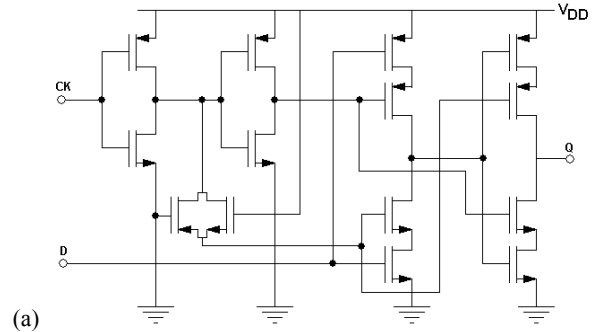


Figure 6. Transistor level DFF used in the divide-by-8 circuit (a) and spice simulation results,  $f_{in}=100$ MHz (b).

### 3.3. Measurements results

The test IC was designed and fabricated according technological design rules of a  $1.5\mu\text{m}$ , 2P2M, N-well, 5-V CMOS process. Figure 7 shows a photo of the fabricated IC, where it can be observed the complete DPLL circuit along with the independent test circuits. Each basic circuit has an output buffer to handle the input capacitance of the oscilloscope probes. Figure 8 presents the comparison output frequency vs control voltage between fabricated ICs and simulation results. A maximum deviation of 8.53% is presented, which can be considered as an acceptable error because, in practice, the VCO will be used into its linear region, i.e. voltages lower than 3V. We expect our students can test every block of the DPLL under several test conditions, being one of the most important the logic performance at low voltage levels. The reason is simple, digital circuits can work at voltages as low as 1.1V to minimize power consumption. Thus, if some additional circuit requires major voltage operation a DC-DC voltage converter can be used, i.e. a  $\times 2$  voltage generator. Finally, Figure 9 shows experimental results captured by an HP Infinium oscilloscope off the frequency division given by the circuit divider when it is connected at the VCO’s output. Such response is the correct one.

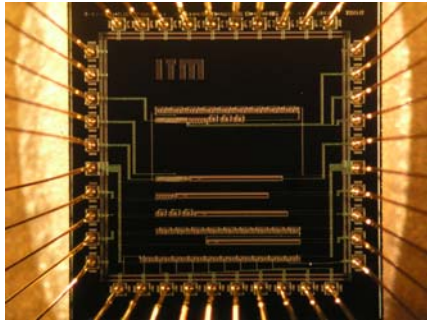


Figure 7. Fabricated test IC. The added buffers were designed to deliver a load of 15pF.

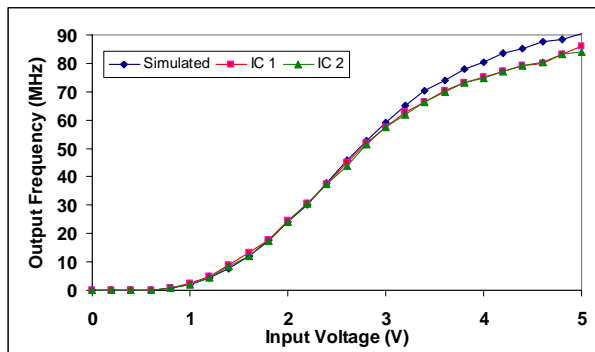


Figure 8. CMOS ring oscillator performance: measured vs simulation.

#### 4. CONCLUSIONS

With the rapid growth and evolution of the microelectronics technology, it is important that students in our universities learn about modern CMOS IC design, simulation and test. With the use of “educative oriented” IC’s, as the one presented here, undergraduate students in the ITM are now starting to relate with the subject, and now there are a student group who has initiated digital and mixed-signal IC design based on standard cells. As a result, students gained knowledge of CAD tools and about the modern IC design and test process. Nevertheless, the use of open source or free software can be frustrating at times to new users. The group need to invest more time to analyze all the mentioned possibilities and decide which CAD tool fit to our needs, and helps to reduce design cycle time.

In particular, students of the PLL design course have now a real IC application of their course theory, which can be tested in their laboratory sessions. We believe that other courses of the curricula could benefit with this kind of projects as well. It is important to underline that universities and also research centers could join us to share experience, knowledge and common objectives to improve the education provided in our universities. From this first IC experience

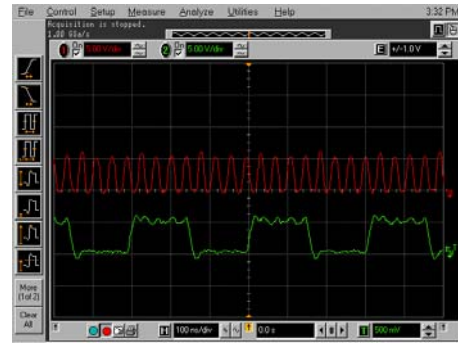


Figure 9. VCO/Divide-by-8 test oscilloscope screen.

with undergraduate students, an IC formed by a Digital PLL frequency synthesizer was fabricated in a 1.5 $\mu$ m, 5-V CMOS technology. It was also tested and first experimental results have been presented here. This IC is the first one designed in any academic institution of the so-called Maya-region.

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