MILLER OTA DESIGN USING A DESIGN METHODOLOGY BASED ON THE GM/ID AND EARLY-VOLTAGE CHARACTERISTICS: DESIGN CONSIDERATIONS AND EXPERIMENTAL RESULTS

Fernando Paixão Cortes, Sergio Bampi

Federal University of Rio Grande do Sul (UFRGS) – Informatics Institute
Caixa Postal 15.064 – Zip 91.501-97 – Porto Alegre, RS - Brazil

{fpcortes, bampi}@inf.ufrgs.br

ABSTRACT

*Analog circuit design is a challenging activity because the analog design procedure targets complex design specifications that are closely related to transistor sizing and device technology dependent. This paper addresses the design of CMOS Miller Operational Transconductance Amplifier (OTA) using a design methodology based on the g_m/I_D characteristic with some new features, including to the design method phase an additional phase: choosing the transistor lengths (**L**) to minimize power. The analog module was analyzed, designed and prototyped in AMS0.35µm CMOS technology. Experimental results are presented, in order to validate the methodology.*

1. INTRODUCTION

The development of ultra-scaled *VLSI* technologies, coupled with the demand for more signal processing integrated in a single chip, has resulted in a tremendous potential for design of analog circuits. Most *VLSI* systems require analog sub-systems such as amplifiers, comparators, filters, oscillators, digital-to-analog and analog-to-digital converters.

The objective of analog circuit design is to map signal conditioning constrains into electronic circuit blocks that meet those specifications. This task is a challenging activity because the analog design procedure targets complex design specifications like dynamic range, noise, offset voltages, gain, etc. These parameters are closely related to transistor sizing, device technology dependent and in particular make the digital environment a harsh condition for meeting analog S/N ratios and dynamic ranges.

Most often the analog design process imposes design trade-offs, some of them taken based on designer's experience with that technology to achieve a successful design. More critical in deep sub-micron CMOS mixed-signal ICs are the specifications of analog circuits that are sensitive to the random variations of the size and technology parameters.

This work focuses on the analysis, design and implementation of CMOS Miller Operational Transconductance Amplifier (OTA) using the $\boldsymbol{g_m/I_D}$ design method. In this method, we consider the relationship between the $\boldsymbol{g_m/I_D}$ ratio and the normalized drain current $\boldsymbol{I_D/(W/L)}$ as a fundamental design relationship to explore the design space. In addition to that, we added an optimization in the design phase: choosing the transistor lengths (***L***) to minimize power. In order to accomplish that, we consider another important characteristic related with the $\boldsymbol{g_m/I_D}$ curve: the relationship between $\boldsymbol{g_m/I_D}$ versus ***VA*** (the Early Voltage parameter).

In [1] [2] [3] several analog blocks, including the Miller OTA, were designed using this methodology. The design procedure aimed best performances in terms of dc gain (***Av***), phase margin (***PM***) and slew rate (***SR***), showing good results. Preliminary simulations results shows that a conventional design approach achieves a similar performance with similar area, hence incurring in much larger power dissipation than that obtained in the $\boldsymbol{g_m/I_D}$ method. The process parameters were obtained through electrical simulation considering the AMS0.35µm CMOS technology.

This paper is organized as follows: Section 2 addresses the design methodology and its main features in detail. The application of the methodology in the design of a Miller amplifier is presented in detail in Section 3. Section 4 presents a quick overview of the prototyped test chip where the amplifier was implemented. The experimental results of this implementation, including comparison with simulation results, are shown in Section 5. Finally, Section 6 presents our conclusions.

2. GM/ID BASED DESIGN METHODOLOGY

Most methods for analytical synthesis of analog circuits suppose that the MOS transistors are either in strong inversion or in weak inversion. The design methodology based g_m/I_D characteristic, proposed by [4], allows a unified synthesis methodology in all regions of operation the MOS transistor.

In this method, we consider the relationship between the ratio of the transconductance g_m over the DC drain current I_D, and the normalized drain current $I_D/(W/L)$ as a fundamental design relation to be explore in the design space.

The choice of g_m/I_D is based on its relevance for the following reasons:

- It is strongly related to the performance of analog circuits;
- It gives an indication of the device operation region;
- It provides a simple way to determine the transistors dimensions.

Considering that the g_m/I_D ratio and the normalized current $I_D/(W/L)$ are independent of the transistor sizes [3], the relationship between them represent a unique characteristic for all transistors of the same type (NMOS and PMOS) in a specific technology.

This "universal" quality of the g_m/I_D versus $I_D/(W/L)$ curve can be exploited during the design phase, when the transistors aspect ratios (***W/L***) are unknown. Once the value of the g_m/I_D ratio is chosen, i.e., the device operation region is determined, the ***W/L*** of the transistor can be determined in the curve.

For each analog block the designer has to deal with a fixed power (or current) budget. Then, with the drain current desired – normally at a maximum level set by power or bandwidth constraints - the ***W/L*** ratio of each transistor can be found.

In addition to the discussed design method, we included an additional optimization in the design phase: choosing the transistor lengths (***L***) to minimize power. In order to accomplish that, we consider another important characteristic related with the g_m/I_D curve: the relationship between g_m/I_D versus ***VA*** (the Early Voltage parameter). This relationship is considered as a fundamental device technology relation that determines the minimum allowable transistor lengths. Once the values of the g_m/I_D ratio and ***VA*** parameter (that is directly related with the transistor output resistance, and consequently with the stage DC gain) are chosen, the ***L*** of the transistors can be determined in our methodology.

Considering both characteristics, the design procedure consists in two basic phases. First, the ***W/L*** of each transistor is found through the g_m/I_D vs. $I_D/(W/L)$ curve. Then, the transistor lengths (***L***) are found considering the g_m/I_D vs. ***VA*** curve.

Both curves were obtained through electrical simulations for the AMS0.35µm CMOS technology, and several analog blocks, including the Miller OTA, were designed using this methodology, as described in [1] [2]. In the next section, we explain the proposed design methodology more clearly, using as a case of study the OTA Miller design.

3. APPLYING THE GM/ID METHODOLOGY IN THE DESIGN OF A MILLER OTA

The proposed methodology was applied to the synthesis of a Miller Operational Transconductor Amplifier (OTA), a two-stage operational amplifier with a feedback capacitor. Figure 1 shows the amplifier schematics.

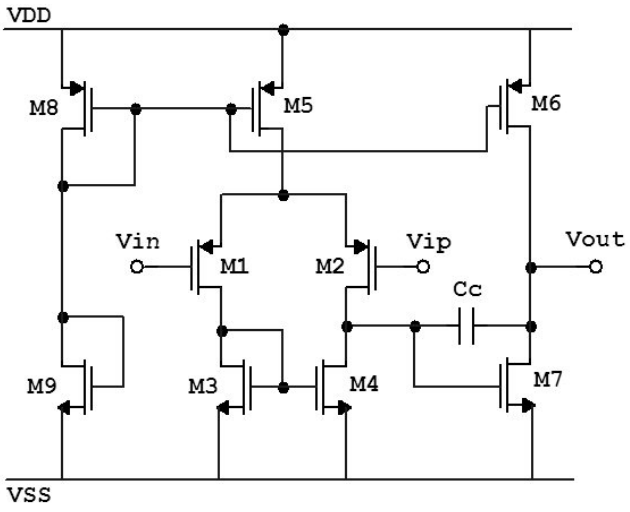

Figure 1 - Miller OTA schematics

The specifications of the design of the Miller amplifier, based on [1] [2] [3], are enumerated in Table 1

Table 1 – Miller OTA design specifications

	Specs
Av (dB)	> 80
PM (°)	60
GBW (MHz)	15
SR (V/μs)	18
I_{DD} (A)	< 325.5
ICMR (V)	-0.5 to 1
Output load CL (pF)	10

First, it's necessary to choose the value of the compensation capacitor ***Cc***. From the specified phase margin, the value of ***Cc*** is chosen, i.e., for a 60° phase margin we use the following relationship:

$$Cc > 0.22 \cdot C_L \Rightarrow Cc = 2.5pF \qquad \text{(eq. 1)}$$

The value of the bias current (***Ibias***) is determined based on the slew rate requirements (in this case we chose an ***Ibias*** of 45 μA.

Thus, the next step is to obtain the transistor sizes do meet the require specifications. The complete design procedure is demonstrated as follows.

3.1 Design phase 1: choosing the W/L for each transistor

Considering the design specifications and their effect in the amplifier performance [5], the values for g_m/I_D are chosen, and then the normalized current $I_D/(W/L)$ is determined for each transistor from the g_m/I_D vs. $I_D/(W/L)$ curve for the target technology (previously obtained in [1] [2]). Then, with the drain current value found, the ***W/L*** of each transistor can be obtained.

This design phase is illustrated as follows:

- the current mirror transistors (M3-M4) are operated in strong inversion to guarantee good matching and noise properties. Thus we choose $(g_m/I_D)_3 = (g_m/I_D)_4 = 10 \rightarrow (W/L)_3 = (W/L)_4 = 10$;
- considering the ***GBW*** specification, the g_m/I_D ratio of the NMOS differential pair (M1-M2) can be determined: $(g_m/I_D)_1 = (g_m/I_D)_2 = 10.47 \rightarrow (W/L)_1 = (W/L)_2 = 36$;
- from the relation $g_{m7} \geq 10 \cdot g_{m1}$ [5], we determine the size of M7: $(g_m/I_D)_7 = 10 \rightarrow (W/L)_7 = 61.8$;
- considering the transistors are operating in moderate inversion, $(g_m/I_D)_5 = (g_m/I_D)_6 = (g_m/I_D)_8 = 7 \rightarrow (W/L)_5 = (W/L)_8 = 30$, $(W/L)_6 = 158$.

3.2 Design phase 2: choosing the L for each transistor

Considering the g_m/I_D values obtained in the previous design phase and the design specifications, the minimum allowable transistor lengths can be obtained based on the ***VA*** parameter that is directly related with the transistor output resistance, and consequently with the stage DC gain.

Considering the Miller OTA analysis based on [3], we can obtain the following equations for the DC gain ***Av*** as a function of the g_m/I_D ratio and ***VA***:

$$Av1 = -\left(\frac{gm}{ID}\right)_2 \cdot \left(\frac{VA2 \cdot VA4}{VA2 + VA4}\right) \qquad \text{(eq. 1)}$$

$$Av2 = -\left(\frac{gm}{ID}\right)_7 \cdot \left(\frac{VA6 \cdot VA7}{VA6 + VA7}\right) \qquad \text{(eq. 2)}$$

where $Av = Av1 \cdot Av2$.

Now, considering the previous analysis and the DC gain specification, we can obtain the length for each transistor. This design phase is illustrated as follows:

- in order to guarantee good matching and noise properties in the differential pair (larger area), the length of each transistor is chosen, $L_1 = L_2 = 3\mu m$;
- considering the g_m/I_D vs. ***VA*** curve, the correspondent ***VA*** can be found: $VA1 = VA2 = 151.6$ V;
- considering the DC gain spec, L_1 and $VA1$, the current mirror ***VA3*** can be obtained through equation 1 $\rightarrow VA3 = VA4 = 10.2$;
- considering the g_m/I_D vs. ***VA*** curve, now the correspondent ***L*** can be found: $L_3 = L_4 = 0.6\mu m$;
- the same procedure is follow considering equation 2 $\rightarrow L_5 = L_6 = L_8 = 1\mu m$ and $L_7 = 0.6\mu m$.

The final values of the g_m/I_D ratio and the transistors sizes are shown in Table 2.

Table 2 – Miller OTA transistor dimensions obtained through the design methodology

Transistor	g_m/I_D	W/L	W (μm)	L (μm)
M1	10.47	36	108	3
M2	10.47	36	108	3
M3	10	10	6	0.6
M4	10	10	6	0.6
M5	7	30	30	1
M6	7	158	158	1
M7	10	103	62	0.6
M8	7	30	30	1.5
M9	1	0.25	1	4

4. TEST CHIP PROTOTYPE OVERVIEW

A test chip with several analog blocks and test vehicles, including the designed Miller OTA, was implemented and prototyped in AMS 0.35μm CMOS technology [1] [2].

Figure 2 shows the die photography of the test chip, where the total area shown is about 4.55 mm².

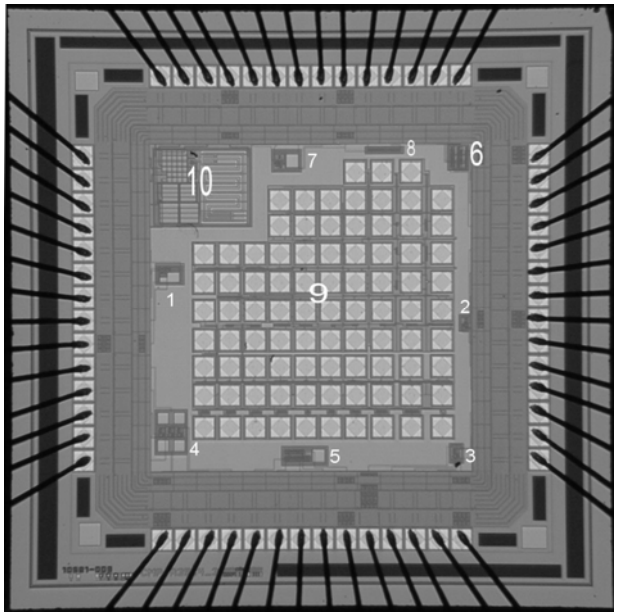

Figure 2 – AMS 0.35μm Test Chip microphotography

Table 3 gives an overview of all blocks that composes the test chip, including the PADs (which were obtained from the AMS0.35um technology library). Each building block and test structure were

Table 3 - Blocks that composes the test chip.

Block		**Area (μm²)**
1	Miller OTA - Ver. 1	83 x 119
2	Comparator	41 x 70
3	OTA	56 x 82
4	GM-C Band-Pass Filter	90x70
5	Miller OTA TAT - Ver.1	77 x 198
6	Comparator TAT	93 x 108
7	Miller OTA - Ver.2	90 x 125
8	Ring Oscillator	29 x 165
9	Test Structures	1100 x 1150
10	Band-gap	300 x 400
Total Area		**2134 x 2134**

The chip microphotograph of the Miller amplifier is shown in Figure 3. The compensation capacitor was fixed at 2.5pF, and laid out as a double-poly capacitor. In this way, the non-linear gate capacitance effects will not interfere in the amplifier performance. The output stage M6-M7 and ***Cc*** dominate the total area. The total active area of the OTA is 3,784 μm² (without the Miller capacitance).

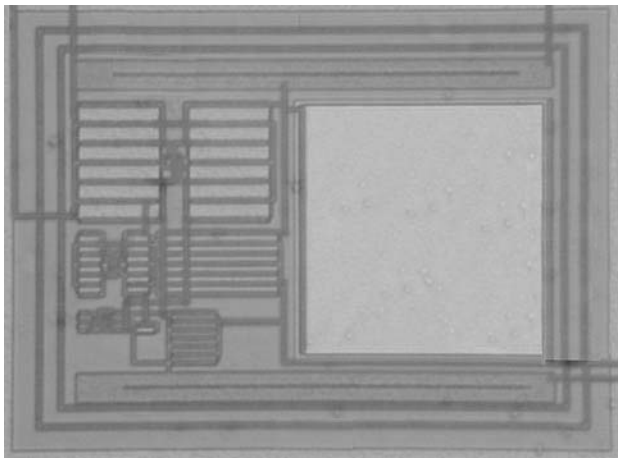

Figure 3 – Chip microphotography of the Miller OTA

5. EXPERIMENTAL RESULTS AND COMPARISONS

The implemented Miller amplifier was fully characterized through electrical measurements from the mentioned test chip.

In order to obtain the experimental results, the average of measurements of 5 samples for the test chip is considered. All the simulated and measured values are for a 20 pF load.

Figures 4 and 5 shows the measured results of the open-loop frequency response (Bode Diagram) and the step response (unity gain configuration) of the amplifier, respectively.

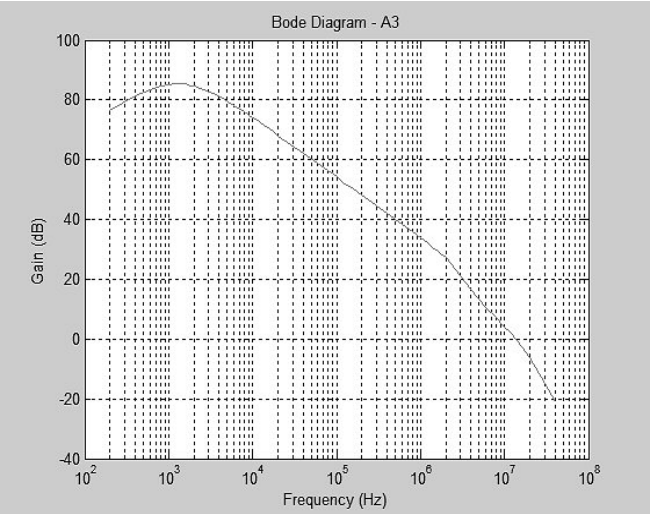

Figure 4 - Measured frequency response for the OTA Miller

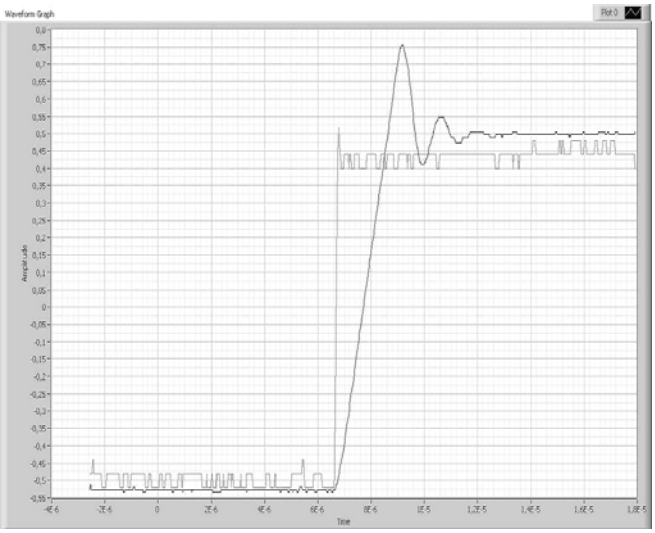

Figure 5 - Measured step response for the OTA Miller

In order to further demonstrate the interest and potential of the methodology, we also compare its experimental results with the results obtained from the electrical simulation using the Spectre simulator and BSIM3v3 transistor model for the AMS 0.35µm CMOS technology. Table 3 shows an overview of the obtained amplifier performance (simulated and measured).

Table 3 - Comparison of simulation and experimental results of the OTA Miller performance

	Electrical Simulation	**Experimental Results**
Av (dB)	85.42	78.5
GBW (MHz)	15.19	12.7
PM (º)	60.07	45
SR (V/µs)	9	3.52
Settling time (ns)	-	812.8
Offset voltage (mV)	-	2.48m
ICMR (V)	-0.52 /+1.45	+0.95/-1.54
CMRR (dB)	89.9	90.4
V_{out} range (V)	+0.9 to -1.4	+1.58 to -1.51
I_{DD} (µA)	339.4	259.9
Power (mW)	0.93	0.86

The design procedure aimed best performances in terms of: dc gain (***Av***), phase margin (***PM***) and slew rate (***SR***). Our results show that this design approach achieves good performance results, showing good matching between simulation and experimental results.

However, there are significant decreasing in the gain bandwidth product (***GBW***), phase margin (***PM***) and slew rate (***SR***) performances in the experimental results. This is due to the larger parameter variation for short channel devices in the prototyped samples. Also, the current source (a resistor implemented by a NMOS transistor) and output load (from the test setup) variations can contribute to decrease the circuit performance.

6. CONCLUSIONS

A design methodology based on the $\boldsymbol{g_m/I_D}$ characteristic with some new features was presented in this paper. An additional optimization is made in the design phase: choosing the transistor lengths (**L)** to minimize power.

The analog module Miller Operational Transconductance Amplifier was analyzed and designed with the parameters and methodology proposed, showing good simulation and experimental results, demonstrating the capability of the proposed methodology, aiming fast analog designs with high level of automation. However, the performance in the experimental results was deteriorated for some parameters, due to the larger process parameter variations. Also, the current source and output

load variations contributed to decrease the circuit performance.

As future work, we intend to study and the effects of noise and ***THD*** (Total Harmonic Distortion) in the design methodology, mostly in the transistor ***L*** choose design phase. The Miller amplifier topology will be considered first in this method. Considerations about the layout of the design blocks, including matching effects in the performance will be also addressed. Then, this methodology will be also automatized and applied in the design of several analog blocks considering different applications [6].

7. ACKNOWLEDGEMENTS

The support of CNPq and CAPES Brazilian agencies with scholarships and PDI-TI Program grant are gratefully acknowledged.

8. REFERENCES

[1] F. P. Cortes, E. Fabris, S. Bampi, "Analysis and design of amplifiers and comparators in CMOS 0.35µm technology", *Microelectronics Reliability,* Eselvier Ltd., April 2004, vol. 44, p. 657 – 664.

[2] F. P. Cortes, E. Fabris, S. Bampi, "Applying the Gm/ID Method in the analysis and design of Miller amplifier, comparator and Gm-C filter" *IFIP VLSI-Soc 2003*, Poster Session, Germany, December 2003.

[3] A. G. Girardi, F. P. Cortes, L. S. de Paula, S. Bampi Design Using Trapezoidal Association of MOS Transistors. Proceedings of IFIP VLSI-Soc 2005, Perth, Australia, October 2005.

[4] F. Silveira, D. Flandre, P. G. A. Jespers, "A gm/ID Based Methodology for the Design of CMOS Analog Circuits and Its Application to the Synthesis of a Silicon-on-Insulator Micropower OTA". *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, September 1996.

[5] Allen, Phillip E.; Holberg, Douglas R. *CMOS Analog Circuit Design*. Oxford University Press, 2002.

[6] Fabris, Eric E.; Carro, Luigi; Bampi, Sergio. A. *An Analog Signal Interface with Constant Performance for SOCs.* IEEE ISCAS2003. May, 2003.