Verification of I/O Buffers Using a Modified Oscillation Technique

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***Abstract*— Variations of slew rate (SR) and simultaneous switching noise (SSN) cause signal integrity loss. Thus, a BIST strategy to verify them is proposed using oscillation-based test principles. Two completely digital sensors are proposed to monitor SR variations and if SSN is greater than an established value, respectively. The sensor outputs control the VCO oscillation frequency allowing to monitor SR and SSN variations. A counter converts the VCO oscillation frequency to a digital value. This is modified when SR changes or SSN is greater than the established value. Monitoring this digital value, the proposed system determines if a buffer has a fault. Results show that the proposed verification strategy is able to detect SR variations of $\pm 10\%$ and SSN of 0.52 V with 100 ps of width.**

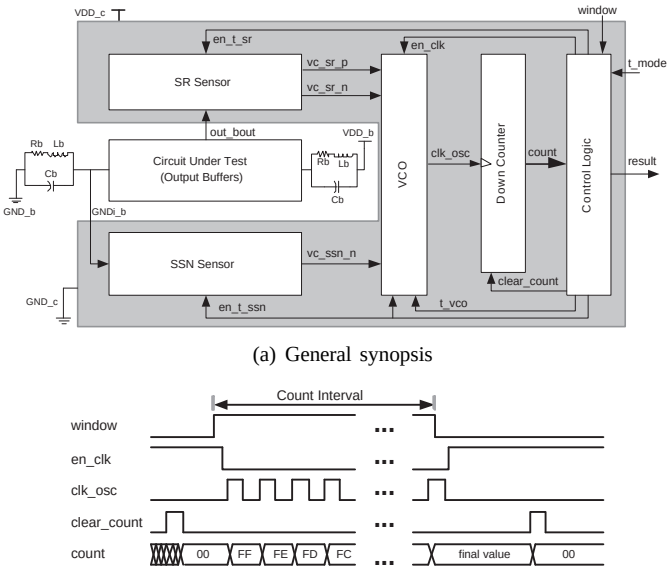
I. Introduction

Higher data transmission rate (6.4 GB/s [1]) and lower voltage supply do signal integrity issues in buffers are more important in deep-submicron technology. Thus, design specifications for buffers become more complex [1]–[3]. Reliability is one of most important requirements. As a result, designers have to take process variations into account in the performance of proposed buffers [1], [4].

Variations of time specifications in the range of tens of ps are significant actually [1]. These variations may be caused by the SR or SSN. A change in the SR ($SR = I/C_L$) produces variations of the propagation delay, rise and fall time, crosstalk, and power consumption modifying the current (I). On the other hand, SSN produces a voltage drop (V_m) through the effective parasitic inductance (L) associated to power network ($V_m = Ldi/dt$) [5]. This change in voltage supply causes variations in time domain, and it can cause an incorrect transmission or reception data if the SSN level is higher than an allowed value or can cause the distortion of output waveform and the circuit may not achieve the performance specifications [2].

BIST strategies were reported for testing I/O buffers [1], [6], [7], but anyone verifies SR. For monitoring SSN in deep-submicron technology, analog sensors have been proposed [8]–[10], but they need a voltage supply different to what buffers use. In this work, a BIST strategy to verify SR and SSN variations is proposed using completely digital sensors. This propose uses principles of oscillation-based test (OBT) [11].

This paper is organized as follows. Section II describes the used methodology. The sensors are presented in Section III and the simulations results are analyzed in Section IV. Finally, Conclusions are given in Section V.



(a) General synopsis

(b) Waveforms of signals controlling the strategy

Fig. 1. Proposed strategy

II. General Verification Methodology

Using OBT, the circuit under test (CUT) oscillates and its oscillation frequency allows to know if it has a fault or not [11]–[13]. In this case, oscillation stability and an adequated sensitivity of the oscillation frequency respect to the fault have to be guaranteed. This work proposes to use two completely digital sensors for translating the SR and SSN variations produced in the CUT to voltage signals which determine the oscillation frequency of a voltage controlled oscillator (VCO) (see Figure 1(a)). Enabling a down counter during a count interval established by the signal *window*, the VCO oscillation frequency is converted to a digital value, *count* (see Figure 1(b)). For a given count interval, the value of *count* when the count interval ends depends on the VCO oscillation frequency.

SR sensor receives the output of a buffer (*out_bout*) and establishes the waveform of the control voltages *vc_sr_n* and *vc_sr_p* according to the SR in each rising and falling edges, respectively. The VCO oscillation frequency is modified according to changes in the waveform of the VCO control signals.

SSN sensor receives the internal ground of buffers (*GNDi_b*) and establishes the value of *vc_ssn_n* according to the maxi-

mum amplitude of the voltage in *GNDi_b* (see Figure 1(a)). SSN sensor has a threshold value that can be adjusted during its design. If the amplitude of *GNDi_b* is always lower than this threshold value, *vc_ssn_n* has the value of VDD, and the VCO oscillation frequency is the expected. In contrast, when the amplitude of *GNDi_b* becomes higher than the established threshold value, the value of *vc_ssn_n* decreases from VDD, and the VCO oscillation frequency is different to the expected.

In order to reduce the influence of the SSN produced by the CUT in the verification system behavioral, CUT is powered through the pines *VDD_b* and *GND_b* and the verification system through the pines *VDD_c* and *GND_c* (see Figure 1(a)).

The VCO and the counter operate as an ADC because they convert the VCO oscillation frequency to a digital value. Its resolution is given by Equation 1 [10] where T_{win} is the count interval in s and K_{vco} is the VCO gain in Hz/V.

$$1LSB = \frac{1}{T_{win}K_{vco}} \tag{1}$$

According to Equation 1, the resolution improves when the count interval increases. In [10] used a count interval of 500 ns. This work presents results with count intervals of 300 ns, 400 ns and 500 ns.

Process variations may change the final count value. Thus, control logic has to take them into account establishing a range of allowed final count values for SR verification as well as SSN verification. This range is established according to what levels of SR o SSN variations are considered as a fault which depends on design specifications. Control logic can change the range of allowed values modifying the comparison values.

Phase noise and jitter in the VCO is no critical for this technique [10] because its average frequency during the count interval is what determines the final count value.

Externally, the verification system receives the signal *t_mode* to know if it operates in test mode or normal mode. When *t_mode* is $'1'$, verification system does all proposed strategies in this work, and when *t_mode* is $'0'$, verification system allows the normal operation of all of buffers.

The VCO is formed by 15 inverter gates *INV_OSC* (see Figure 2). Each one has two parallel pMOS and two parallel nMOS. One of these is controlled by SR sensor and the other by SSN sensor, but they are not used simultaneously. Their gate voltage establishes their propagation delay, and thus, the VCO oscillation frequency. In this way, variations in the SR or SSN change the VCO oscillation frequency and the final count value.

The counter is an 8 bits down ripple counter. The used flip-flops are formed by two static latches and can run at 1 GHz. Their largest transistors has an aspect relation of $W/L = 1.26/0.18$.

In order to improve the sensitivity in relation to a SR or SSN fault, output buffers have to be stimulated with a digital signal whose frequency is the highest that achieves a rail-to-rail output. In this work, the frequency of the stimulus at the input buffers is 625 MHz (1600 ps of period) and it is an external signal.

The proposed verification system was designed in the TSMC 0.18 um technology.

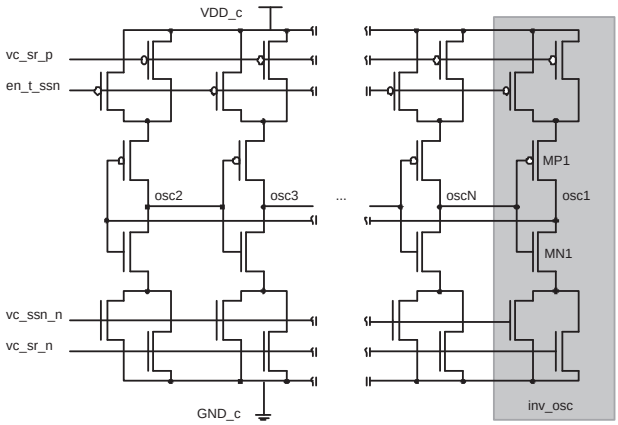


Fig. 2. Basic VCO structure

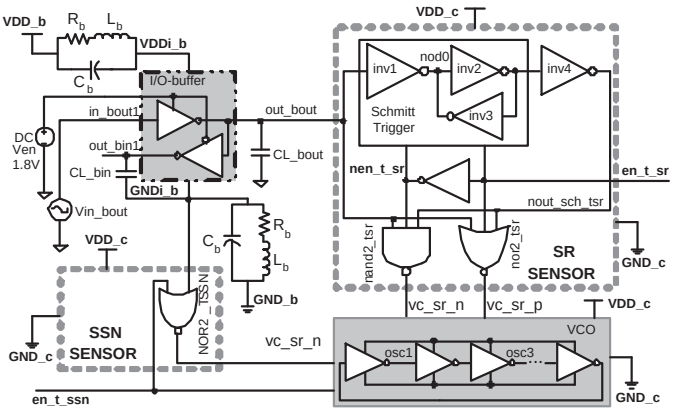


Fig. 3. Proposed sensors for verifying SR and SSN

III. Sensing Circuitries

Proposed sensors are completely digitals and they are implemented using conventional CMOS logic for achieving more noise immunity. SR sensor is made up by a schmitt-trigger, a NAND, and a NOR gate; and SSN sensor is made up by a single NOR gate. They are connected to the output buffer as Figure 3 shows. A SR sensor is required for each buffer but only one SSN sensor is required for all buffers powered through the same VDD and GND pines.

A. SR sensor

SR sensor uses the rise and fall times to monitor the SR. It has an enable signal called *en_t_sr* that has to be $'0'$ to operate. The NAND gate generates *vc_sr_n*, and the NOR gate generates *vc_sr_p*.

At the beginning of a rising edge, *nout_sch_tsr* (see Figure 4) and *vc_sr_n* are both at $'1'$ logic. When the SR sensor is enabled, the logic value of the *vc_sr_n* depends on *out_bout* (see Figure 4). When *out_bout* reaches the value of V_{th_nand}, the NAND gate begins to discharge its output node. This succeeds until *out_bout* reaches the value of $V_{thH\_schmitt}$. When this occurs, *out_bout* is $'1'$ and *nout_sch_tsr* is $'0'$, and then the NAND gate begins again to charge its output node. According to this, the reached minimum amplitude by *vc_sr_n* in each rising edge depends on the value of $t_{r0} =$

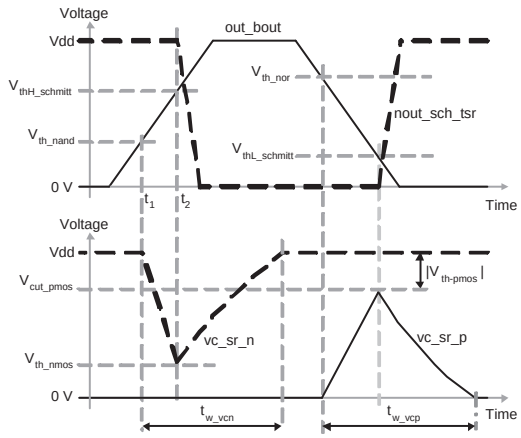


Fig. 4. Generation of the SR sensor outputs

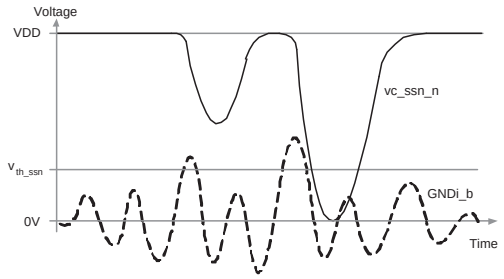


Fig. 5. Generation of the SSN sensor output (*vc_ssn_n*)

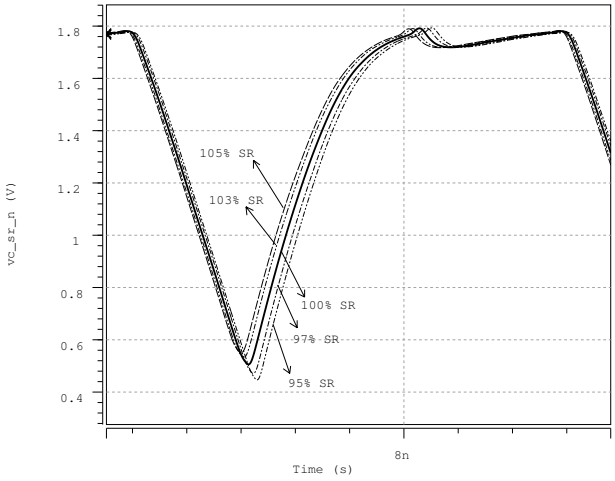
$t_2 - t_1$ (see Figure 4). When the SR increases, t_{r0} decreases, and the minimum amplitude of *vc_sr_n* increases. When the SR decreases, t_{r0} increases, and the minimum amplitude of *vc_sr_n* decreases. When the minimum amplitude of *vc_sr_n* changes, its width of pulse changes too. Both changes are caused by SR variations and modify the VCO oscillation frequency. The pulse of *vc_sr_p* is generated in similar way but in each falling edge.

In this work, the threshold voltage of the NAND and NOR gates are 0.6 V and 1.19 V, respectively, and for the schmitt trigger are 0.3 V and 1.34 V.

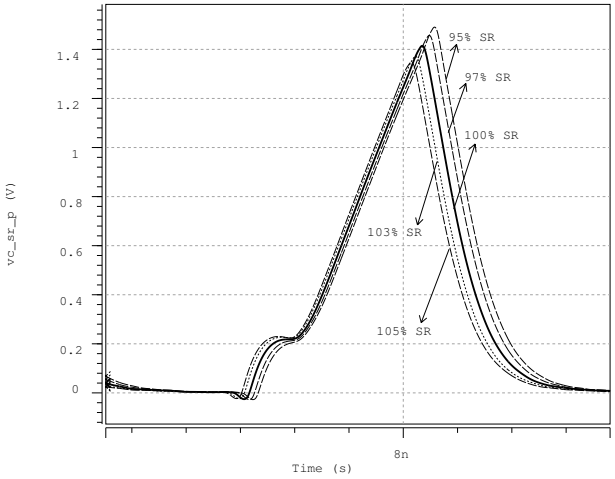
B. SSN sensor

SSN sensor establishes the waveform of its output according to the value of the amplitude of *GNDi_b* (see Figure 5). When the amplitude of *GNDi_b* is lower than the threshold voltage of the SSN sensor, *vc_ssn_n* has the value of VDD. Each time that the amplitude of *GNDi_b* is greater than this threshold voltage, the amplitude of *vc_ssn_n* decreases from VDD. How much it decreases it depends on how much the amplitude of *GNDi_b* is greater than the threshold voltage of the sensor and the width of that pulse. Figure 5 shows this; the second pulse of *vc_ssn_n* is greater that the first one because the amplitude of *GNDi_b* in the second is greater than in the first. The threshold voltage of the designed SSN sensor is 0.48 V which can be adjusted.

Because the threshold voltage of a pMOS is greater than of a nMOS, this work proposes to measure the amplitude of voltage in the internal node GND instead of the amplitude in the internal node VDD.



(a) *vc_sr_n*



(b) *vc_sr_p*

Fig. 6. Real waveforms of the outputs given by SR sensor output (*vc_sr_n* and *vc_sr_p*) affected by slew rate of the output buffer

IV. Results

All simulations were done in HSPICE with TMOS model level 49. The power pines (VDD and GND) of the CUT and of the system verification contain a RLC net, where $R_b = 0.1$ Ω, $C_b = 0.1$ pF and L_b can be 0.2 nH, 0.6 nH or 1.0 nH, and the external voltage sources used for them are different. Count intervals of 300 ns, 400 ns and 500 ns were used. The buffers are stimulated with a digital signal with a period of 1600 ps in order to improve their sensitivity to faults.

A. Verification of the SR

For this test, SSN sensor has be disabled and only one of the SR sensors has to be activated. The SR is varied $\pm 10\%$ around its nominal value. The Figure 6 shows the real waveform of the outputs given by SR sensor, *vc_sr_n* and *vc_sr_p*, with variations of SR from 95% to 105%. The minimum amplitude and the pulse width of *vc_sr_n* and the maximum amplitude and the pulse width of *vc_sr_p* are modified when the SR

TABLE I
COUNT VALUES FOR VARIATIONS OF THE SR IN THE RANGE OF $\pm 10\%$

% of SR	Count in 300 ns	Count in 400 ns	Count in 500 ns
90.0	168	139	110
91.0	167	137	108
92.0	166	136	106
93.0	164	134	103
94.0	163	132	102
95.0	162	131	99
96.0	162	130	99
97.0	162	130	99
100.0	**160**	**128**	**96**
103.0	157	124	91
104.0	156	123	90
105.0	156	123	89
106.0	155	122	88
107.0	155	121	88
108.0	155	121	88
109.0	154	120	86
110.0	154	120	86

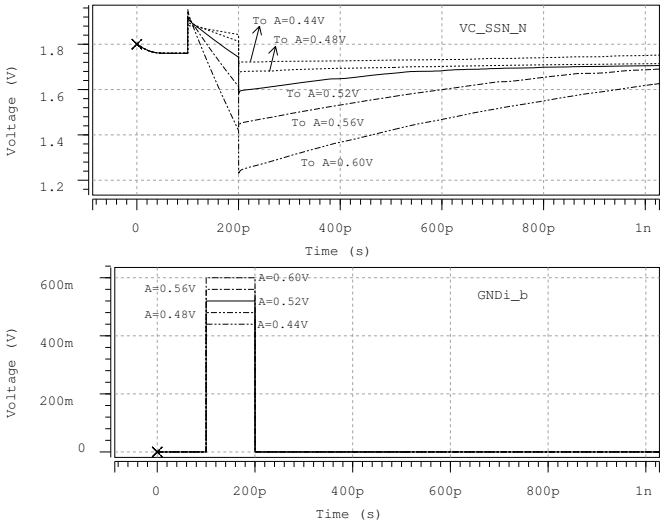


Fig. 7. Sensitivity of the SSN sensor

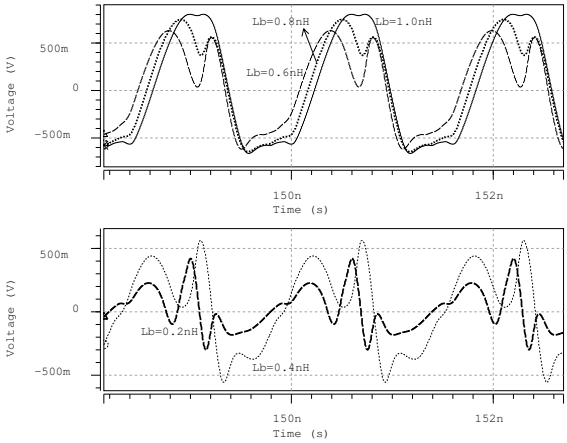
changes. This changes are the responsibles of the variation in the final count value.

Table I lists the count values obtained in the tests of the SR. The values of the SR goes from 90% to 110% of its nominal value (100%). The expected count value for each count interval corresponds to the case of 100% of the SR. When the SR is different to its nominal value, the count value is different to expected value. The difference between the expected count value and the count value for different SR values increases when the SR value is more different to its nominal value and when the count interval increases as the Equation 1 indicates.

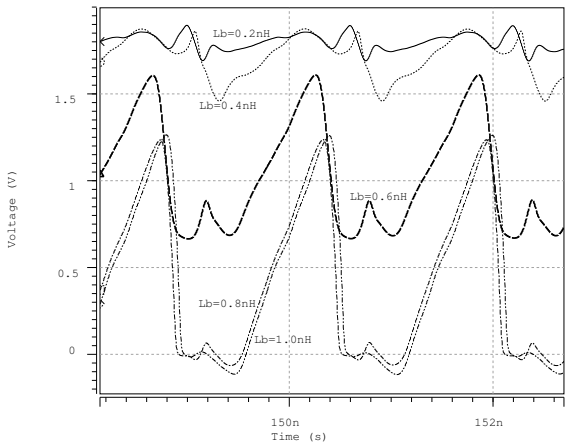
These results show that the proposed verification system is able to monitor variations of the SR of $\pm 10\%$ of variation.

B. Verification of the SSN

For this test, all SR sensors are disabled and the SSN sensor is activated. Values of 0.2 nH, 0.6 nH and 1.0 nH for the parasitic inductance are used. The considered number of buffers switching simultaneously are 2, 4, 6, 8 and 10.



(a) Internal ground of output buffers (*GNDi_b*)



(b) Output given by the SSN sensor (*vc_ssn_n*)

Fig. 8. Real waveforms in the SSN sensor with 10 output buffers switching simultaneously

The sensitivity of the SSN sensor is tested stimuling it with pulses of width of 100 ps and amplitudes from 0.44 V to 0.60 V with steps of 0.04 V. Figure 7 shows that SSN sensor varies significantly its ouput from a amplitude of 0.52 V.

Figure 8 shows real waveforms of the internal ground of the output buffers and the output of the SSN sensor *vc_ssn_n*. When the value of L_b is higher, the level of SSN is higher too. The difference among the waveforms showed in the Figure 8(a) is less than among the waveforms showed in the Figure 8(b). This shows that the SSN sensor has an adequated selectivity.

Table II lists the count values obtained in the tests of the SSN. The expected count value for each count interval corresponds to the case of $L_b = 0.0$ nH. The count value increases from the expected value when the number of buffer switching simultaneously and the value of L_b increases. This is appreciated from the number of buffers is greater or equal to 4. With $L_b = 0.6$ nH, the count value is significantly different to the nominal value from 8 output buffers switching simultaneously, and with $L_b = 1.0$ nH, from 4 output buffers. With $L_b = 0.2$ nH, the count value is the nominal in all cases. The difference between the count value and the nominal value increases when the count interval increases as the Equation 1 indicates.

TABLE II

COUNT VALUES IN VERIFICATION OF SSN FAULTS WITH 2, 4, 6, 8 AND 10 OUTPUT BUFFERS SWITCHING SIMULTANEOUSLY

Number of output buffers	L_b $[nH]$	Count in 300 ns	Count in 400 ns	Count in 500 ns
	0.0	**125**	**81**	**37**
2	0.2	125	81	37
	0.6	125	81	37
	1.0	125	81	37
4	0.2	125	81	37
	0.6	125	81	37
	1.0	126	82	39
6	0.2	125	81	37
	0.6	125	82	38
	1.0	174	147	119
8	0.2	125	81	37
	0.6	129	86	44
	1.0	209	194	178
10	0.2	125	81	37
	0.6	160	128	96
	1.0	209	193	177

V. CONCLUSIONS

The results show the feasiblity of the proposed modified oscillation technique to verify SR and SSN violations at the I/O buffers.

The use of VCO as means of oscillation allows not to add requirements to the buffers design that they could add if the buffers would oscillate.

Two completely digital sensor have been proposed to verify the SR and the SSN produced by buffers. The SR sensor is formed by a schmitt-trigger, a NAND and a NOR gate. The SSN sensor is only formed by a NOR gate. The design specifications is simple to obtain. The proposed sensors do not depend on the buffer architecture and do not specific characteristics of a technology. The proposed SSN sensor does not depend on the pin or package model, because of that this sensor can be used with others pin or package models.

The results show that the proposed verification system can monitor variations of the SR of $\pm 10\%$ and the level of SSN of 0.52 V of amplitude. The resolution of the strategy improves when the count interval increases.

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