Efficient Approach to Realize a Very- Low-Frequency Filter

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Abstract – **An area-efficient switched-capacitor filter technique to perform large time-constant is described. The technique allows obtaining very large time constant by increasing the number of stages in the switched-capacitor topology. The filters have been used to implement an experimental 100 rad/s filter controlled by 100KHz clock frequency.**

Keywords — **Switched-Capacitor, low–frequency, large-time-constant.**

I. INTRODUCTION

Passive filters contain inductors and capacitors that provide linear-polynomial approximations of ideal filters. Corner frequencies generally range from hundreds of Hertz to many mega-Hertz. However, low-frequency passive filters are large and heavy, and manufacturing them is expensive. Input signals undergo "insertion loss" (attenuation) at DC. Magnetic-material non-linearity makes building low-distortion filters of this type difficult. Also, since passive filter circuits use inductors, they are not easily programmable. The realization of large time-constant filter circuits have two properties that make their production in monolithic IC form difficult, these are the need for large-value capacitors and resistors. Several approaches have been investigated to develop large time constant by using active configurations [1,2], but little has been made in the development of passive filters of low frequency. In this regard, the method of filter design that would lend to IC implementation is the switched-capacitor filter technique. Switched-capacitor techniques eliminate external component requirements and allow a clock-tunable cutoff frequency (the ratio of the clock frequency to the low-pass cutoff frequency can be internally set to desire value). In addition, VLSI technology (generally CMOS) has facilitated complete integration of switched-capacitor circuits on a single monolithic chip. In the present work, we describe an efficient approach for switched capacitor technique to perform very-large time-constant with it's analytical verification and electrical simulation.

II THEORETICAL ANALYSIS

In order to realize a low frequency filtering (very-large time-constant filter) is suitable to use the technique of switched capacitor. A switched capacitor filter simulates resistor as switched capacitors. The basic topology has problem with the accuracy due to the parasitic capacitance. The parasitic or stray capacitance appears from the switch nodes to ground. These uncontrolled strays can add significant capacitance to the typical configuration of switched capacitor. These strays will be affecting the accuracy of the filter response. In order to minimize this effect will be necessary to modify the typical configuration as is showed in Fig. 1. In this way, the simulated resistor becomes immune to the surrounding strays.
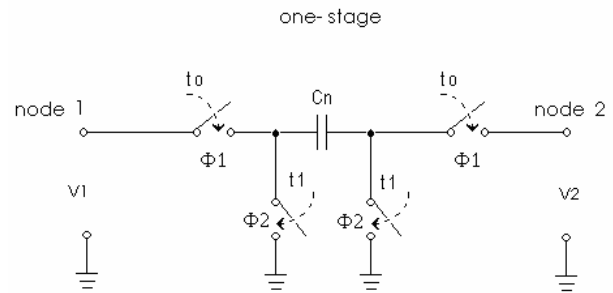

Fig. 1. Switched-Capacitor "Resistor".

In t_o , the switch $\Phi 2$ closes while switch $\Phi 1$ is opening, in t_1 switch $\Phi 1$ closes while the switch $\Phi 2$ is opening, then transferred a charge is transferred from V_1 to V_2, the emulated resistance R_{eq} is,

$$R_{eq} = \frac{T_c}{C_n} \qquad (1)$$

where T_c is the filter sample period, [s], and C_n is the capacitance value, [F]. The technique is based on assumption of switched-capacitor-resistor equivalence, in which the result is correct if $f_c = \infty$ while is approximately correct if $f_c \gg$ work frequency. This assumption is a good factor which influences the complete performance and determines the clock frequency in very low frequency switched-capacitor filter. The emulated resistance for the previous configuration (Fig. 1) with node 2 connected to capacitor Ce, gives RC time constant τ as,

$$\tau = \frac{1}{f_c C_1} C_e \qquad (2)$$

where C_e is the value of the integration capacitor. From the switched capacitor equation (2), in this case it follows that the absolute value of the corner frequency depends on the ratio of two capacitors, not on their absolute values. Similarly, analyzing several stages (two and three), we can obtain the analytical solution for the emulated resistance as follow,

$$R_{eq} = \frac{T_c}{C_{eq}} \qquad (3)$$

being $\frac{1}{C_{eq}}$ equal to with equal to $\sum_{n=1}^{i} \frac{1}{C_i}$. For instance, a plot of log R_{eq} versus C1 is shown in figure 2 for three, two and one stages. The considered values were: 10 µs for filter sample period and switched capacitors C3 equal to 0.1pF and C2 equal to 0.1pF.
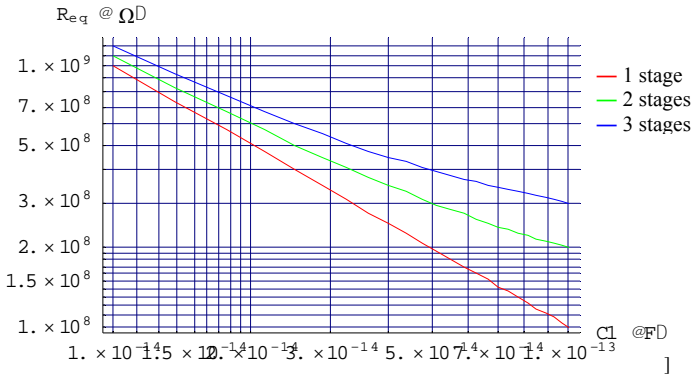

Fig. 2   Comparison of R_{eq} for different stages.

These analytical results show the increase of emulated resistance. For the same value of the capacitance C1, it is possible to obtain 200 MΩ of increase (between three and one stage. Although the emulated resistance is greater when the capacitance begins to diminish, this alternative is not preferred because these capacitances (smaller than 50fF) bring problems of nonlinearity and distortion.

In conventional switched-capacitor structures, the required capacitor ratios tend to be huge, typical values of f_c (clock frequency) 100 kHz to 100 MHz with values of C_i = 0.1 pF to 10 pF gives values of R_{eq} = 1 kΩ – 100 MΩ [3]. However, in the design of integrated capacitor the result would be quite large. For the biggest capacitor (10 pF) with poly-poly2 layers (0.5 micron CMOS processes), the resulting area is about 106.9 µm per side. Furthermore, if we are looking a cutoff frequency smaller than 100 Hz, the previous topology is not a good alternative, we will need for the best case (f_c= 100KHz, C_i =0.1 pF) a $C_e \approx$ 100 pF or another option will be reevaluate the switched capacitor value. Both alternatives have important disadvantages: increase the required areas and cause nonlinearity and distortion. Therefore, the option that circumvented the traditional way of switched capacitor circuit would be

necessary. Maintaining the low values of the elements (capacitors, resistors) and to uphold the typical range values of f_c, by increasing the number of stages in the simple topology. Thus, for fully integrated filters with very-large constant time, therefore, the proposal is to introduce as much number of stages. In a simple approximation, for a time-constant τ = 0.01 s, will be needed an emulated resistor of R_{eq} =1 GΩ. For two stages i=2 (refers to Fig. 2), a charge $C1\dfrac{V1-V2}{T_c}$ is transferred from C1 to C2 that is equal to $C2\dfrac{V2-V3}{T}$. In this section we consider the frequency response of a switched-capacitor filter. The filter circuit consists of a resistor (for instance, the emulated resistance giving by C1 and C2) and a capacitor in series C_e with the input signal V1. Solving the differential equation for boundary condition V1 equal to a constant, it can be shown that the s-domain transfer function of this approach is given by

$$H_2[s] = \frac{k_2}{(s+k_2)} \qquad (4)$$

being k_2 equal to $\dfrac{C_{eq}}{C_e} f_c$.

The output of the circuit is taken to be the voltage across the capacitor C_e. This voltage across the capacitor tends towards V_{in} as time passes. The constant time is the time required to charge the capacitor through the resistor to 63.2 ($\sim$ 63) percent of full charge (cyan abscissa axe) of its initial voltage, which can be determinates empirically with a plot of V output versus time as showed in figure 3. The 63% is marked with cyan abscissa axe.
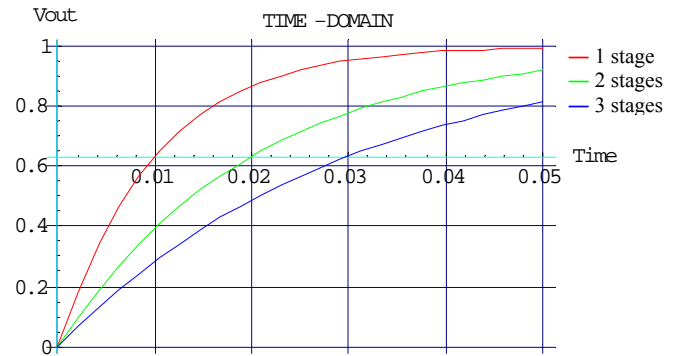

Fig. 3 Time-domain response for 1, 2 and 3 stages for V_{in} equal to 1 and C_e equal to 100 pF.

The determined cut-off frequencies for 1, 2 and 3 stages were: 100 rad/s, 50 rad/s and 33 rad/s respectively. These results show larger time constant, τ due to the emulated resistance R_{eq} is bigger for the topology greater stage.

In the frequency-domain, the analytical result for transfer function gives the frequency response showed in figure 4.
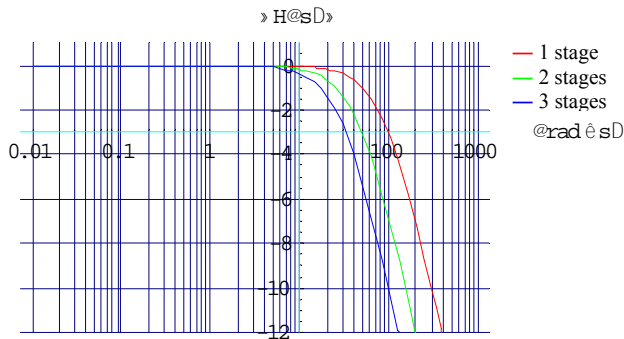

Fig. 4. Frequency response for 1, 2 and 3 stages with C_e equal to 100 pF.

At the same way, the results for the cut-off frequencies are verified: 100 rad/s, 50 rad/s and 33 rad/s for 1, 2 and 3 stages respectively.

In addition, for the second and third stage was made a second calculation to fit the cut-off frequency to 100 rad/s; for 2-stages, the value of C_e, was reduced to 50 pF, and for 3-stages the reduction was to 33.3 pF.

III. ELECTRICAL SIMULATION RESULTS

A simple RC low-pass filter was considerate although switched-capacitor filters in practice are opamp based. But we consider that the simple RC circuit illustrates the feasibility of the approach described.

TopSpice demo software was used for the simulation of switched-capacitor topologies. Running the simulations for 3, 2 and 1 stages we obtain the time-domain response of emulated resistor R_{eq} equal to 100 MΩ; the output voltages at V(SC1), V(SC2) and V(SC3) show a slope, however the switched-capacitor output rises in a stair-stepped waveform. Results of simulation are summarized in Fig. 5. For the three topologies, the frequency responses are plotted in dB from a range of frequency from 1 to 400 rad/s.
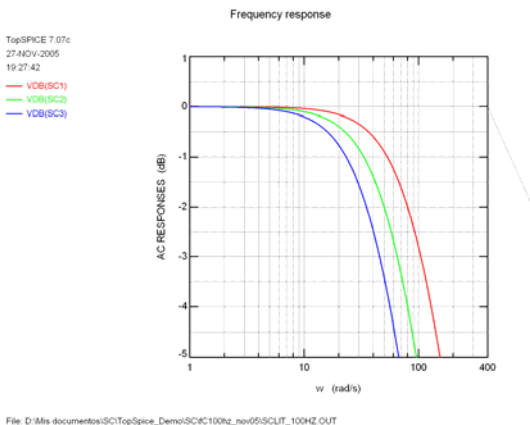

Fig. 5. Frequency response of topologies 1, 2 and 3 stages.

Figure 5 shows for each topology, the frequency at which the closed-loop magnitude response is equal to -3dB. Looking at the plot, we find that it is approximately 100 rad/s for 1 stage. For 1 to 2 stages, we obtained a frequency shift of 40 rad/s, whereas of 2 to 3 stages, the frequency shift was of 20 rad/s. On increasing the stages, this frequency start to shift to lower values, indicating changes in the time constant of each topology (with the same value of C_e). Consequently, if the switched-capacitor stage is increased, R_{eq} must be increased proportionately.

For more than 3 stages, we have limitations of demo software due to maximum number of data points (must be less than 16000).

IV. CONCLUSION

The study of low frequency filters by using a simple technique has been presented. Cutt-off frequencies were obtained by comparison of 1, 2 and 3 stages. The time- and frequency-responses of the simulated and analytical filters give similar results. The technique allows decrease the capacitor value by increasing the number of stages of the topology, therefore by increasing the number of stages in the switched capacitor circuit, a very large time-constant is obtained. The results could be used to prove the feasibility of the proposal.

ACKNOWLEDGMENT

V. REFERENCES

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