PHOTOGATE ACTIVE PIXEL SENSOR MODELING USING PSPICE

Victor H. Ponce-Ponce, Felipe Gómez-Castañeda, José A. Moreno-Cadenas
Ezequiel Molinar-Solis and Herón Molina-Lozano

E-mail: vponcep@ipn.mx
UPIITA-IPN
Av. IPN, No. 2805, C.P. 07360, Mexico City, Mexico

Abstract – **Photogate-type pixels are structures widely used in the design of modern CMOS integrated cameras, but also in real-time CMOS vision sensory system applications. This work introduces a PSpice macromodel for CMOS photogate-type active pixel sensors that can be used for electrical simulation. The aim of this work is to introduce a PSpice macromodel due to the lack of macromodels reported in the literature. Simulation results as well as measurements of a test photogate-type active pixel sensor, fabricated in a standard CMOS process, N-well, using 1.2 microns, design rules are presented.**

1. INTRODUCTION

CMOS active pixel sensors (APS) technology is emerging as an alternative in the solid-state imaging technology with respect to the charge couple device (CCD) technology, because it has significant advantages in terms of reduction in the development and fabrication costs. Power dissipation, scaling to high resolution formats and compatibility with camera-system integration are also important aspects in CMOS APS technology [1].

In the design flow of a CMOS APS, the use of macro models for simulation of devices capable of being fabricated in standard CMOS IC processes is an important issue. An analysis of photocurrent models for some photodetector devices has been reported [4] and PSpice macromodels for the photodiode detector can be found in the literature [5], however, there is a lack of macromodels reported in the literature of photogate-type CMOS APS, for simulation tools like PSpice.

2. CMOS PHOTOGATE PIXEL

A cross-section of a photogate (PG) in a P-substrate is shown in Fig. 1. A PG is a MOS capacitor that is exposed to light. When a positive voltage (*VG*), is applied to the polysilicon gate, photo generation of carriers is produced in the depletion region which is formed under the gate and in the neutral region. During the integration time (T_{int}), photons pass through the polysilicon gate and generate hole-electron pairs. Holes are expelled from the depletion region to the substrate, due to the developed electric field in the depletion region. On the other side, electrons are attracted by the gate and are accumulated in the silicon surface, underneath the gate. The PG is biased positively, typically at V_{DD}, thereby creating a potential well in the deep-depleted substrate. This is why the MOS capacitor can be seen like a bucket which can be filled with charges; see Fig. 2(a-c). A transmission gate, M4, is used to transfer charges from the PG potential well to the floating-diffusion diode (FD) node where charge-to-voltage conversion is done due to its associated depletion capacitance (C_{FD}). The voltage change (δV) at the FD can be expressed as:

$$\delta V_{FD} = N_e \frac{qG_{pix}}{C_{FD}} = N_e C_{VF} \qquad (1)$$

Where δV_{FD} is proportional to the number of electrons (N_e) accumulated with time, in the PG potential well. G_{pix} is the gain voltage of the in-pixel source follower transistor M2, and C_{VF}, is defined as the charge-to-voltage conversion factor (in V/electron). A reset transistor M1, is used to reset the FD. The source voltage of M2 can be selected and read by using a pass transistor M3, which generally connects the source terminal of M2 with a common-column external load transistor for reading the pixel signal.

One drawback of a PG structure is that it has a poor blue spectral response, since the gate absorbs most of the short wave-length visual spectrum. Even more, in modern CMOS IC processes, silicides components are added to the gate to reduce contact and sheet resistance, blocking almost all the visual spectrum. Some solutions to this problem have been faced by opening some windows on the gate so that light can pass through. In spite of the poor blue response of a PG structure, its C_{VF} grows as the area of the gate terminal increases, compared with the photodiode, where the C_{VF} remains independent of the photodiode area, for a given incident photon flux.

3. OPERATION OF THE PHOTOGATE

The basic sequence of operations for a PG APS are: signal integration, reset and charge transfer. During signal integration, *TX* and *RST* are biased lower than the PG to provide for some antiblooming control, preventing charges from spilling over from a full well, and avoiding to flow into adjacent pixels. See Fig 2(a). After an integration time, *RST* signal is pulsed to V_{DD} to reset the FD to approximately $0.75V_{DD}$. The final reset voltage reached at the FD node is $V_{FD}=V_{DD}-V_{th}$, where V_{th} is the MOSFET threshold voltage. The FD is reset immediately, before the signal readout, because this allows improved noise reduction; see Fig 2(b). Next, *VG* is pulsed to 0V, to transfer the charge throughout M4 onto the FD node. Then δV is read as the corresponding pixel signal; see Fig 2(c).

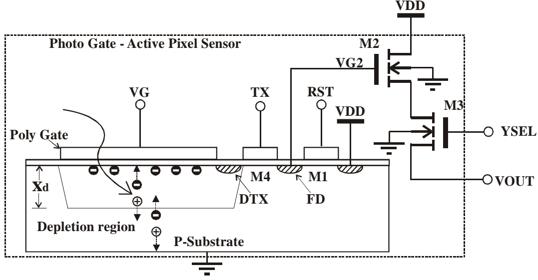

Fig. 1. Cross-section of a photogate-type active pixel, during the photocharge integration period

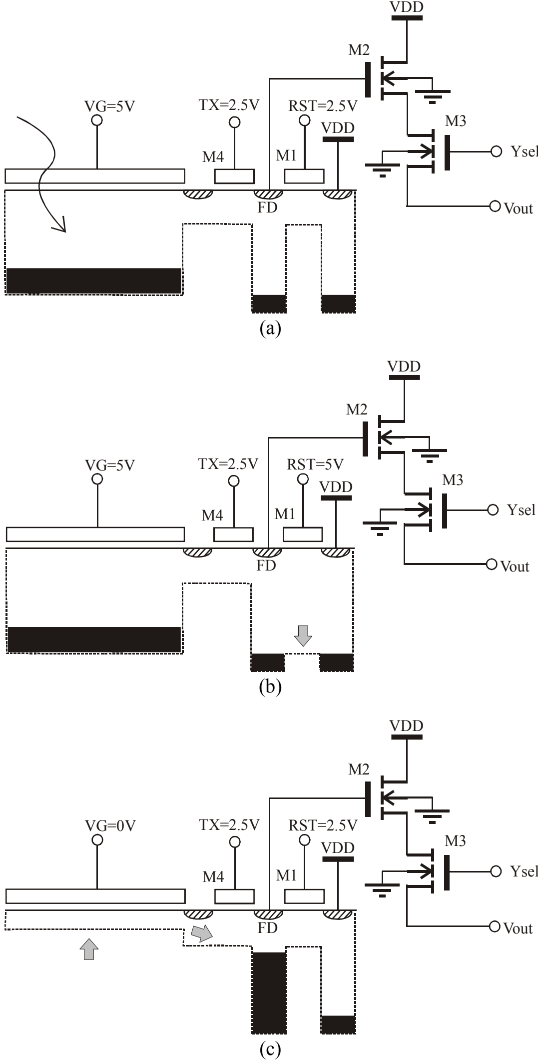

Fig. 2. Sequence of operations for a PG APS (a) time integration, t_{int} (b) Reset period and (c) Charge-transfer and floating-diode potential surface lecture.

4. GENERATED PHOTOCURRENT

For the structure shown in Fig. 1, the generated photocurrent, that fills the potential well, is composed of two components: the drift current, due the drift of holes and electrons in the depletion region and the diffusion current (I_{DIFF}), due to the diffusion of photocarriers outside the depletion region. Only the current component due to diffusion is considered, since the depletion region width (X_d) is very thin for modern CMOS IC technologies (typically 0.5μm). Short-wavelength photons do not penetrate profoundly inside de substrate and since they are almost completely absorbed by the polysilicon gate material, there is a negligible amount of short-wavelength photons arriving to the thin depleted region to generate photocarriers. Then, it is reasonable to consider that all the charges filling the potential well are diffusing from areas outside the depletion region where longer-wave length photons can penetrate. Therefore, the spectral model of the PG can be obtained by solving the diffusion equation[4], in one dimension, in the neutral region which is formulated as follows:

$$D_n \frac{\partial^2 n_p}{\partial x^2} - \frac{n_p - n_{po}}{\tau_n} + G(x) = 0 \tag{2}$$

where D_n is the electron diffusion constant, n_p and n_{p0} are the excess and equilibrium minority carriers in the P-substrate, respectively, τ_n is the electron life-time and $G(x)$ is the generation rate of hole-electron pairs, due to an incident photon flux arriving at the surface of the substrate per unit area (ϕ_1) given by

$$G(x) = \phi_1 \alpha e^{-\alpha x} \tag{3}$$

where, α is the silicon absorption coefficient and ϕ_1 is obtained by

$$\phi_1 = \phi_o \alpha e^{-\alpha \, Tgate} \tag{4}$$

In (4), T_{gate} is the gate thickness and ϕ_O is the photon flux per unit area arriving to the gate terminal, given by

$$\phi_o = \frac{\lambda P_{inc}(1-R)}{hc} \tag{5}$$

where P_{inc} is the incident light power flux per unit area, R is the reflection coefficient at the gate surface, h is the Planck´s constant, λ the incident light wavelength and c is the speed of light in vacuum. Solving (2), under the boundary conditions $n_p(x)|_{x=xd}=0$ and $n_p(x)|_{x=xd}= n_{po}$, gives:

$$n_p(x) = C_1 e^{\frac{x}{L_n}} + C_2 e^{-\frac{x}{L_n}} + C_3 e^{-\alpha x} + n_{po} = 0 \tag{6}$$

where

$$C_1 = \frac{-n_{po} e^{-\frac{x_{epi}}{L_n}} + C_3 \left[e^{-\frac{x_d}{L_n}} e^{-\alpha x_{epi}} - e^{-\frac{x_{epi}}{L_n}} e^{-\alpha x_d} \right]}{e^{\frac{x_d}{L_n}} e^{-\frac{x_{epi}}{L_n}} - e^{\frac{x_{epi}}{L_n}} e^{-\frac{x_d}{L_n}}} \tag{7}$$

$$C_2 = \frac{-n_{po} e^{\frac{x_{epi}}{L_n}} - C_3 \left[e^{\frac{x_d}{L_n}} e^{-\alpha x_{epi}} - e^{\frac{x_{epi}}{L_n}} e^{-\alpha x_d} \right]}{e^{\frac{x_{epi}}{L_n}} e^{-\frac{x_d}{L_n}} - e^{\frac{x_d}{L_n}} e^{-\frac{x_{epi}}{L_n}}} \tag{8}$$

$$C_3 = \frac{\phi_1 \alpha L_n^{\,2}}{D_n (1 - \alpha^2 L_n^{\,2})} \tag{9}$$

where X_{epi} is the thickness of the epitaxial layer and L_n is the electron diffusion length. The parameter D_n can be computed by using the following empirical expression for silicon, which is a function of the acceptors impurity concentration (N_a) for a P substrate and the temperature (T) [2].

$$D_n = \frac{KT}{q}\left[65.4 + \frac{1265}{1+\left[Na/(8.5\times10^{16})\right]^{0.72}}\right] \quad (10)$$

where K is the Boltzmann's constant and q is the electron charge constant. Parameter L_n is given by

$$L_n = \sqrt{D_n \tau_n} \quad (11)$$

where τ_n is the electron lifetime for silicon and can be obtained by the empirical formula [4]:

$$\tau_n = 1/(3.45\times10^{-12} N_A + 9.5\times10^{-32} N_A^2) \quad (12)$$

The absorption coefficient α, for silicon can be computed with the empirical expression [3]:

$$\alpha = \left(\frac{84.732}{\lambda(\text{in } \mu\text{m})} - 76.417\right)^2 \ \text{cm}^{-1} \quad (13)$$

and the x_d, is computed using [4]:

$$x_d = \frac{-b+\sqrt{b^2+4aV_G}}{2a}, \quad a = \frac{qN_a}{2\varepsilon_{si}}, \quad b = \frac{qN_a T_{ox}}{2\varepsilon_{si}} \quad (14)$$

where ε_{si} is the silicon dielectric permittivity and T_{ox} is the thickness of the thin oxide.

The phocurrent density filling the potential well is obtained by

$$J_{diff} = -qD_n \left.\frac{\partial n_p}{\partial x}\right|_{x=x_d} \quad (15)$$

Finally, substituting (6) in (15), the expression for the photocurrent filling the potential well due to diffusion is

$$J_{diff} = \frac{-qD_n C_1 e^{\frac{x_d}{L_n}}}{L_n} + \frac{qD_n C_2 e^{-\frac{x_d}{L_n}}}{L_n} - qD_n \alpha C_3 e^{-\alpha x_d} \quad (16)$$

5. PSPICE PHOTOGATE MACROMODEL

Using the analog behavioral modeling (ABM) feature of PSpice, equation (16) was used to construct a PSpice macromodel. A GVALUE PSpice part was used to define the photocurrent equation given in Section 4.

The proposed equivalent circuit to model the FD surface potential (δV_{FD}) is shown in Fig. 3.

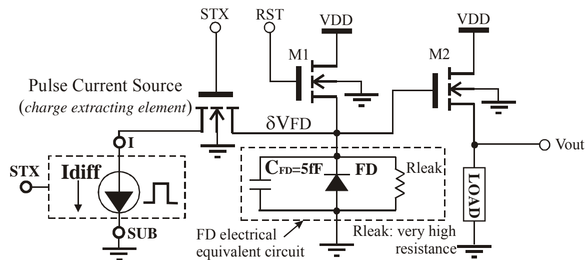

Fig. 3. Electrical equivalent circuit of the PG APS used for simulation, using the *PG* pulse current source subcircuit, *Idiff*.

```
.SUBCKT Idiff  STX  I  SUB
+params: tint=0 tx=0 area=0 pinc=0 vg=0 lambda=0

* (tint)      Photocarge integration-time
* (tx)        Transfer time (it must match the STX pulse width)
* (area)      Photogate area, in [cm^2]
* (pinc)      Incident power of light, per unit area, in [w/cm^2]
* (lambda) Incident light-wavelength, in [um]

* Model parameters (IC process dependent) - - - - - - - - - - - - - - - - - - - -
.param h=6.62617e-34           ; Planck´s constant, in [joules*sec]
.param R=0.0                   ; Reflection coefficient
.param xepi=152e-4             ; Thickness of the epitaxial layer, in [cm]
.param Nd=1e17           ; Electron doping concentration, in [1/cm^3]
.param Na=3.9848e15      ; Holes doping concentration, in [1/cm^3]
.param ni=1.45e10   ; Silicon intrinsic carrier concentration, in [1/cm^3]
.param K=1.38066e-23           ; Boltzmann's constant, in [joules/kelvin]
.param q=1.602e-19             ; Electron charge, in [coulombs]
.param mobp=214.33             ; Surface hole mobility, in [cm^2/v*s]
.param mobn=652.22             ; Surface electron mobility, in [cm^2/v*s]
.param eps=1.035e-12           ; Silicon dielectric permittivity, in [F/cm]
.param c=2.99e14               ; Speed of light in vacuum, in [um/s]
.param Tgate=2e-4              ; Thickness of the poly-gate, in [cm]
.param Tox=0.0319e-4           ; Thickness of the thin-oxide, in [cm]
.param T=300                   ; Room temperature

*Model expressions  - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
.param tn={1/(3.45e-12*Na+9.5e-32*(Na**2))};Elec. lifetime for Si [sec]
.param npo={(ni**2)/Na}        ; Minority carrier concentration, in [1/cm^3]
* Electron diffusion constant, empirical expression for silicon:
.param Dn={((K*T)/q)*(65.4+(1265/(1+(Na/8.5e16)**0.72)))},in [cm^2/seg]
.param Ln={sqrt(Dn*tn)}  ;Electron diffusion length, in [cm]
* Absorption coefficient, empirical expression for silicon
.param alfa={((84.732/lambda)-76.417)**2}; Lambda in [um], but alpha in
[cm].
.param fio={(lambda*Pinc*(1-R)/(h*c))}  ; Optical incident photon-flux
              *{[um*joules/(s*cm^2)/joules*s *um/s]}=>1/(cm^2*s)
.param fio1={fio*exp(-alfa*Tgate)}; photon-flux at the substrate surface

* Model expressions for the diffusion current model - - - - - - - - - - - - - - -
.param Ct1={ (q*Na)/(2*eps) }
.param Ct2={ (q*Na*Tox)/(2*eps) }
.param xd={ (-Ct2+sqrt((Ct2**2)+4*Ct1*Vg))/(2*Ct1) } ; depletion width
.param C3={(fio1*alfa* (Ln**2) )/(Dn*(1-( (alfa**2) * (Ln**2) ) ))}
.param C1num={ -npo*exp(-xepi/Ln)+C3*(exp(-xd/Ln)*exp(-alfa*xepi)-
+                  exp(-xepi/Ln)*exp(-alfa*xd))}
.param C1den={ exp(xd/Ln)*exp(-xepi/Ln) - exp(xepi/Ln)*exp(-xd/Ln) }
.param C1={C1num/C1den}
.param C2num={(-npo*exp(xepi/Ln)-C3*(exp(xd/Ln)*exp(-alfa*xepi)-
+                  exp(xepi/Ln)*exp(-alfa*xd)))}
.param C2den={(exp(xepi/Ln)*exp(-xd/Ln)-exp(xd/Ln)*exp(-xepi/Ln))}
.param C2={C2num/C2den}

.param jtot={abs((-q*(Dn/Ln)*C1*exp(xd/Ln)+
+              q*(Dn/Ln)*C2*exp(-xd/Ln)-
+              q*Dn*C3*alfa*exp(-alfa*xd)))}

.func switch1(Z)={1/(1+exp(-5*(z-2.5)))}
* blocks GPG if STX is in low-state (STX=0V)

.param qint={area*jtot*tint}
*Charge accumulated during integration time (tint)

* Implements the pulse current source
GDIFF I SUB VALUE ={switch1(V(stx))*qint/tx}
*Same charge, transferred when STX is in on-state

.ends Idiff
```

Fig. 4. PSpice subcircuit definition of the pulse current source Idiff, used to model the charge extraction process of the FD node in a PG APS.

The subcircuit has three ports. The ports *I* and *SUB*, correspond to the input-output terminals of the pulsed current generator. A control input port *STX* is used for triggering the pulsed current generator. The time-width of the pulsed signal *STX* must be equal to the parameter *TX* entered in the symbol placed during schematic capture. The PSpice macromodel code for this current generator is introduced in Fig. 4.

6. EXPERIMENTAL RESULTS

The charge-transfer process of electrons stored in the PG potential well to the FD diode, in the last phase of operation of the PG, can be modeled with the use of a current source (I_{diff}) which extracts an amount of charge stored in the FD potential well, after the reset cycle, equal to the accumulated charge (qN_e) in the PG potential well, at the end of the integration cycle. This charge transfer process is assumed to be ideal. A fixed-time pulse width (*TX*) is chosen, then, the subcircuit computes the current amplitude to extract the necessary amount of charge from the FD node.

A fabricated test PG APS, designed for a CMOS vision chip application [6] was used to compare the simulation results of the PSpice macromodel proposed in this work. Some theoretical pixel specifications are shown in Table I.

In Fig. 5, the pixel measured response is shown, under complete darkness, and the corresponding simulation is introduced in Fig. 7.

In Fig. 6, the pixel measured response is shown where a light power incident of P_{inc}= 0.1 mW/cm^2 and light wave-lengh of λ_{inc}=650nm has been applied. The simulation that corresponds to this case is introduced in Fig. 8.

The microphotography of the test cell is shown in Fig. 9.

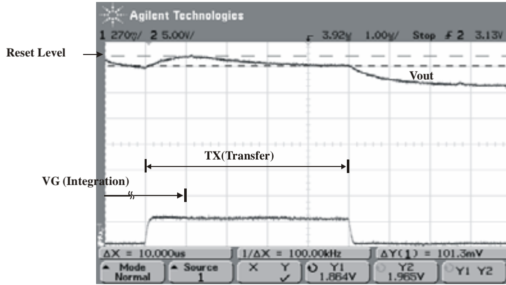

Fig. 5. Pixel measured response in darkness (P_{inc}= 0 mW/cm^2). An integration time of 80µs has been considered

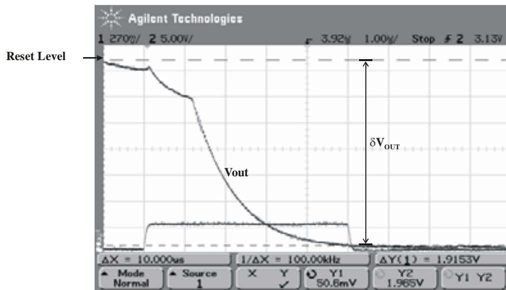

Fig. 6. Pixel measured response under a power incident light of P_{inc}= 0.1 mW/cm^2 and λ_{inc}=650nm. A δV_{out}=1.91V is obtained. An integration time of 80µs has been considered

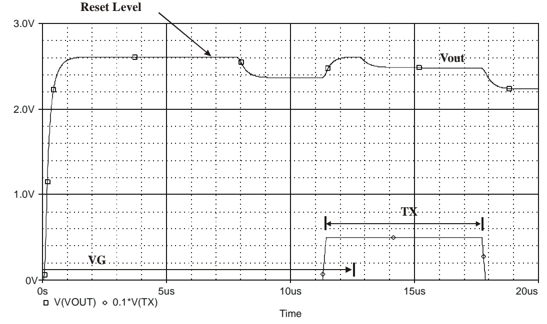

Fig. 7. Pixel simulated response in darkness (P_{inc}= 0 mW/cm^2). An

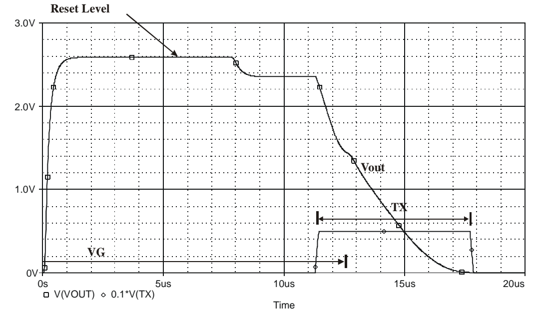

Fig. 8. Pixel simulated response under a power incident light of P_{inc}= 0.1 mW/cm^2 and λ_{inc}=650nm. A δV_{out}=1.91V is obtained. An integration time of 80µs has been considered

The difference in the final V_{out} level obtained after the TX pulse can be attributed mostly to the error in the incident power light measurement at the surface of the integrated circuit. A $P_{inc} \cong 0.1$mW/cm^2 was measured during the test measurement and it was used for the simulation.

TABLE I
GENERAL SPECIFICATIONS

Full-well capacity	49 Me$^-$
FD capacity	144 Ke$^-$
Voltage conversion	27.6 µV/e$^-$
Fill factor	23.6 %

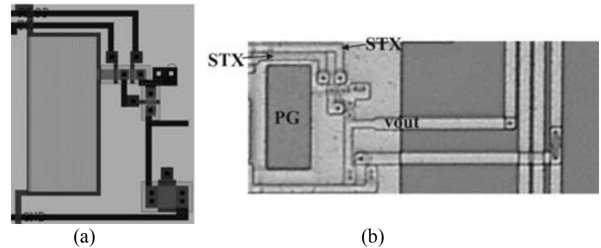

Fig. 9. Photogate (a) layout design and (b) microphotography of the test cell fabricated in standard CMOS double poly and metal, with 1.2 µm design rules

7. CONCLUSIONS

A PSpice macromodel that simulates the photoresponse of a CMOS IC photogate-type active pixel sensor has been presented. The macromodel is based on the analog behavioral modeling (ABM) feature of PSpice. The proposed subcircuit definition contains many parameters that can be easily obtained from CMOS IC data runs. The results of the simulations conducted have been compared with the measurements of a fabricated PG APS test cell, showing a good agreement with the real electrical behavior.

8. ACKNOWLEDGEMENTS

This work was supported by the Center for Research and Advanced Studies (CINVESTAV-IPN) and a grant from the Program SUPERA-ANUIES-COTEPABE, through the National Polytechnic Institute (IPN) of Mexico.

9. REFERENCES

[1] E. Fossum, “Active pixel image sensors―Are CCD’s disnosaurs?,” *Proc. SPIE,* vol. 1900, pp. 2-14, Feb. 1993.

[2] D.M. Caughey and R.E. Thomas, “Carrier mobilities in silicon empirically related to doping and field,” *Proc, IEEE (Lett.)* 55, 2192 (1967).

[3] D. Schroder, “Semiconductor material and device characterization”, *John Wiley and Sons, Inc.*, Ch. 8, 1990.

[4] A. Moini, *Vision Chips*, Kluwer Academic Publisers, 1999, pp. 261-264.

[5] R.J. Perry, K. Arora, “Using PSPICE to simulate the photoresponse of ideal CMOS integrated circuit photodiodes”, *Proc. IEEE SOUTHCON’96*, pp. 374-380, Apr. 1996

[6] Victor Ponce-Ponce, Felipe Gómez-Castañeda, José A. Moreno-Cadenas, Luis M. Flores-Nava, “Motion Detection Sensor Based on CMOS Floating-Gate Devices”, *Proc. ICEEE/CIE*, pp. 206-209, Sept. 2004.