DESIGN OF A 10-BIT 200MS/S CURRENT-STEERING DAC IN 0.13um CMOS TECNOLOGY

J.F. Fernández-Bootello[1], J.A. Segovia[1], A. García-Ortiz[1], A. Rodríguez-Pérez[1], J. Ruiz-Amaya[2], M. Delgado-Restituto[2], F. Medeiro[1,2], and A. Rodríguez-Vázquez[1,2]

[1] AnaFocus [2] Instituto de Microelectrónica de Sevilla – CNM – CSIC – Univ. de Sevilla

medeiro@imse.cnm.es

ABSTRACT

The design of a 10-bit current steering DAC is presented. It employs a fully-differential segmented architecture with 6 thermometric and 4 binary bits. The DAC has been designed in a 0.13um CMOS process and its analog core uses the 3.3V thick-oxide devices available in such technology. The extracted layout has been exhaustively simulated showing correct performance up to 200MSample/s. It consumes 37mA and occupies 0.1mm^2 silicon area.

1. INTRODUCTION

In modern communications system-on-chips, either for base-band or intermediate frequency signal processing (in wireless standards) or for wide-band wireline modems, the digital-to-analog converter has become a ubiquitous functionality.

Current-steering DACs are well suited for these high-speed applications, where they have been proven to be dynamically superior to other techniques such as R-2R resistive division or charge redistribution.

Moreover, the use of optimally segmented topologies, which combine the goodness of the thermometric decoding with the compactness of the binary one, have resulted in small footprint IP blocks with resolutions up to 14bit and sampling rates up to the GHz range. Most of them are compatible with mainstream digital CMOS process and do not require complex calibration algorithms.

Immersed in this trend, we present the design of a current-steering DAC for communication application featuring 10bit@200MS/s in a 0.13um CMOS technology. Section 2 is devoted to the DAC architecture, whose circuitry is described in Section 3. Most important design considerations are outlined in Section 4. Finally, Section 5 compiles some illustrative results.

2. CELL ARCHITECTURE

Figure 1 shows the block diagram of the complete IP cell. Apart from the current-steering DAC, the cell includes a bandgap circuit and reference buffers in order to generate the main bias current and reference voltage to drive the DAC switches. Related signals (*iref*, *vbg*, and *vref*) are brought outside to enable external control and filtering. The differential output is in current mode, thus requiring two external resistors to build the differential output voltage.

The current steering DAC core is composed of 2^{N-1} current sources – N is the number of bits of the digital input words, which steer the current into two resistors as shown in Figure 2. The basic current cell is represented in Figure 3. It is composed of a current source (M_{cs}) and two switches (M_{sw}), which steer the current to the resistors depending on the control signal V_{sw} and its complementary V_{swb}. In order to improve the output impedance of the current cell, these switches work in the saturation region when they are in ON state. To this purpose, the value of switching voltage must be selected to be high enough.

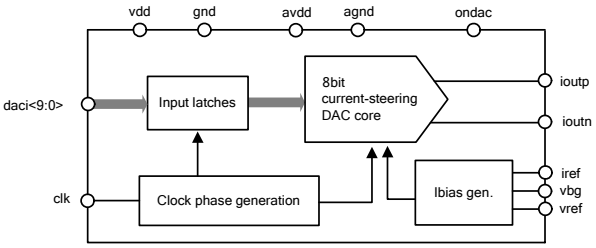

Figure 1 – Block diagram of the DAC cell

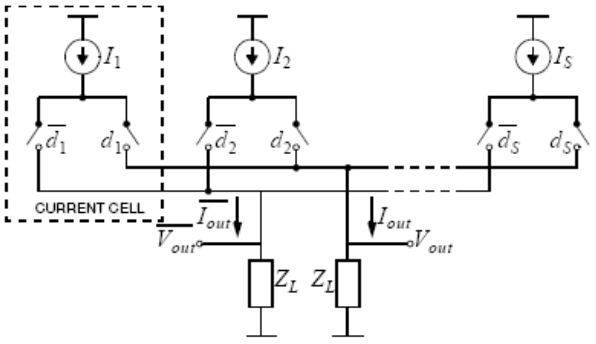

Figure 2 – Conceptual differential-mode current steering DAC

In order to guarantee monotonicity and reduce the influence of glitches, as well as reducing the sensitivity to mismatch errors in small silicon area, current-steering DACs are usually segmented into a coarse and a fine part. This is a common solution for resolutions above ten bits. The coarse part (corresponding to the Most Significant Bits, MSBs) is thermometer-decoded and the fine part is binary-weighted.

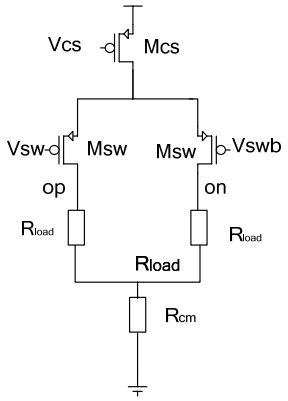

Figure 3 – Basic current source

Figure 4 shows the floorplan of a generic *N*-bit segmented current-steering DAC [1, 5], with *t* thermometer bits and *b* binary bits ($N = t + b$). The total number of cells, S, in the DAC is composed by $S_t = 2^t\text{-}1$ thermometer (or unary) cells and $S_b = b$ binary cells. The nominal output current steered by each of the unary cells is $2^b\, i_0$, where i_0 is the current corresponding to the Least-Significant Bit, (LSB), i.e., $I_{FS}/2^N$. The total current steered by one binary cell is $2^l\, i_0$, were $l = 0, 1, \ldots b\text{-}1$.

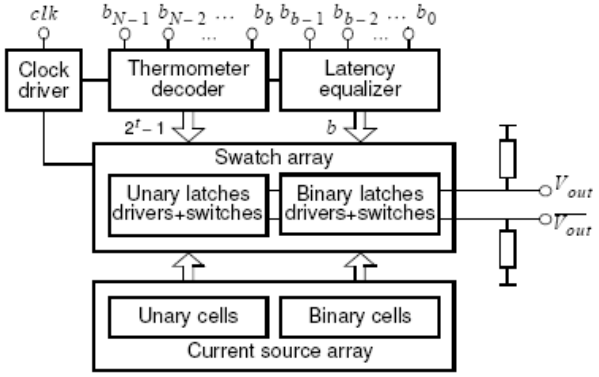

Figure 4 - Block partitioning of a segmented current steering DAC.

When the resolution is high, even if segmentation is employed, the layout of the current source array can take a considerable area. In these conditions, current cells located at the extremes of the array will be very far away and gradient effects will be noticeable. In order to improve the deviation to the ideal characteristics of the DAC produced by gradient errors, the current cells in the layout can be selected using algorithms that minimize such gradients. Among the existing ones, we have selected the so-called Q^2-random walk [2],[3]. It proposes a two level switching. The first one is intended to reduce quadratic gradients, and the second one to reduce linear gradients. The resulting switching scheme for a 10bit current steering DAC is represented in Figure 5. The unary array is divided into 16 quadrants (Q) and each quadrant is divided into 4 sub-quadrants (SQ).

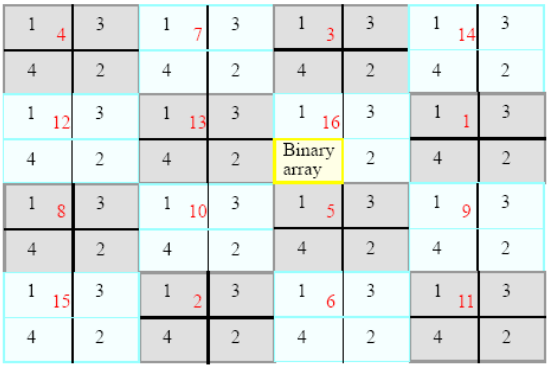

Figure 5 - Switching sequence of the current cells

The order of the switching sequence is as follows: Q1, SQ1 - Q2, SQ1 - ... – Q16, SQ1 - Q2, SQ2 - … - Q16, SQ3. The quadrant 16, sub-quadrant 4 is used for the binary-weighted cells.

3. DESCRIPTION OF THE CIRCUITRY

Apart from the basic current source, already described in previous section, the circuitry required to properly generate the switching voltage (V_{sw}) and current source biasing are described next.

3.1. Digital circuits

The digital part of a segmented current-steering DAC is in charge of translating the input digital words into the switching voltage of the current sources. It begins with a *t* – to – $(2^t\text{-}1)$ thermometer decoder to control de unary current cells and a latency equalizer for the *b* binary bits (Figure 4).

Then, a layer of level shifters is required in order to adapt the logic levels from the 1.2V domain of the digital circuitry to the 3.3V one of the analog core. The level shifter used is shown in Figure 6.

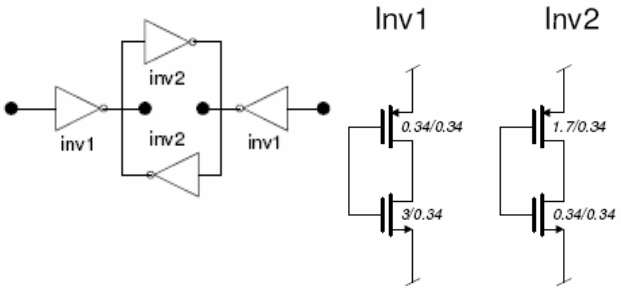

Figure 6 – Digital level shifter

In order to avoid delays between the switching of different current cells, and the subsequent appearance of current glitches, latches like that shown in Figure 7 are inserted immediately after the level shifters [4].

Finally, a couple of inverters commute the gate voltage of the switches between supply (OFF state) and a reference voltage *vref*, which is selected so that the switch transistor operates in saturation region.

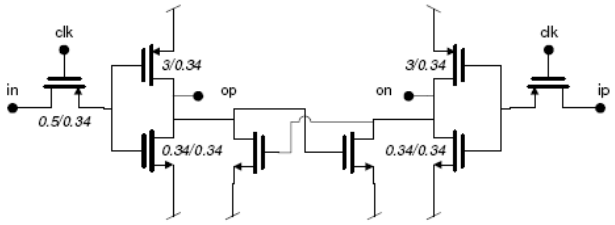

Figure 7 – Synchronizing latch

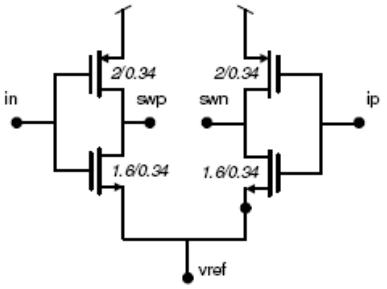

Figure 8 – Switch driver

3.2. Bias circuit

The unary current is generated from an on-chip bandgap voltage. The circuitry involved, shown in Figure 9, utilizes an OTA to form a current-control loop with the help of a nmos and an external resistor. Then, this current is handled by a programmable current mirror so that the full-scale current can be set to either 17 or 34mA. The resulting current is further mirrored to generate the gate voltage of the basic sources.

Also the reference voltage used for turning on the current switches is generated and buffered off-chip for decoupling.

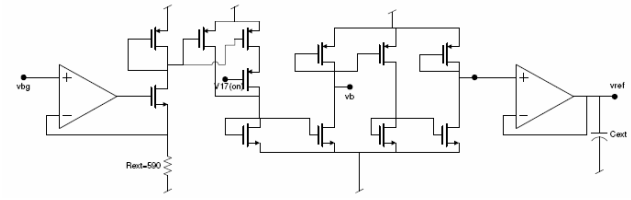

Figure 9 – Bias circuitry (bandgap not shown)

4. DESIGN CONSIDERATIONS

Most important design considerations, related to current source mismatch, output impedance and circuit noise, are covered in the following sections.

4.1. Design of the current source

To design the current source both static and dynamic criteria have to be taken into account. Static performance is usually determined by the Integral Non-Linearity (*INL*). Its worst case value, in the mid code transition, is [1]

$$\sigma_{INL\max} = \sqrt{2^{N-1}}\,\sigma_{i_0} \tag{1}$$

where σ_{i0} is the standard deviation of the mismatch error in the unitary current source. Thus, the σ_{i0} required to get $INL < 0.5$LSB in 99% of cases is

$$\sigma_{i_0} / i_0 = 1/\sqrt{2^{N+1}} / 2.5 \tag{2}$$

In our case, with $N = 10$, the maximum mismatch in the current source becomes $\sigma_{i0}/i_0 \approx 0.9\%$. Since the current mismatch is inversely proportional to the squared root of the transistor channel area, this criterion sets the minimum area of the current device. For the intended technology, the minimum channel area is $WL_{min} = 6\mu m^2$.

Another static feature, the Differential Non-Linearity (*DNL*) depends on DAC segmentation, being determined basically by the number of binary bits [1],

$$DNL^{\max} = (\sigma_{i_0} / i_0)\sqrt{2^{b-1}} \tag{3}$$

The area necessary to achieve the *DNL* specification is usually smaller than the required by the *INL* one.

Dynamic performance is usually mapped to the Spurious-Free Dynamic Range (*SFDR*). An important source of *SFDR* degradation is related to the output impedance of the unary current cell. This renders the output current signal-dependent resulting in harmonic distortion for sinusoidal inputs. For fully differential current cells, *SFDR* is given by [1]

$$SFDR = 40\log_{10}(R_o / R_L) - 12(N-2) \tag{4}$$

where R_o is the output resistance of the current source and R_L is the load resistance. For *SFDR* = 60dB, the resistance ratio must be higher than 10^4, from DC to the application bandwidth.

4.1. Circuit noise

Most important circuit noise contribution is found in the current bias generation circuit because its noise power is mirrored 2^N-1 times to the output. Accounting only for thermal noise, it can be demonstrated that the total output noise power spectral density is signal-dependent,

$$S_o(f) = \frac{16}{3} kTR_L{}^2 \left[(2^N - 2k)^2 i_0 \left(\frac{1}{V_{SAT}} + \alpha\right) \frac{i_0}{i_B} + 2^N \frac{i_0}{V_{SAT}} \right] \tag{5}$$

where k is the input code, i_0 is the unary current, i_B is the biasing current (i_0/i_B is then the current mirror gain), $V_{SAT} = (V_{GS}\text{-}V_T)$ is the saturation voltage of the transistors and α is a factor depending on the currents in the bias transistors and their saturation voltages. The worst-case noise is obtained for either $k = 0$ or $k = 2^N$-1. Assuming a current mirror gain equal to unity, (5) can be simplified to

$$S_o(f) \approx \frac{16}{3} kTR_L{}^2 2^{2N} i_0 \left(\frac{5}{V_{SAT}}\right) \tag{6}$$

Note that $2^N i_0 R_L$ equals the full-scale output voltage amplitude, also called output compliance, V_{cpc}. Hence, we can derive a compact expression for the maximum Signal-to-Noise Ratio (*SNR*) or Dynamic Range (*DR*):

$$DR \approx i_0 / \left[\frac{32}{3} kT \left(\frac{5}{V_{SAT}}\right) \Delta f \right] \tag{7}$$

where Δf is the signal bandwidth and an input sinewave of amplitude equal to V_{cpc} has been assumed. In our design, i_0 = 33.2uA, which for V_{SAT} = 0.7V and Δf = 5MHz, results in 73.2dB DR.

5. ILLUSTRATIVE RESULTS

The current-steering DAC has been designed up to the layout level in a 0.13um CMOS technology. The DAC core utilizes the 3.3V thick-oxide devices available in that technology, whereas all digital circuits have been synthesized using a 1.2V standard cell library. However, the DAC has been proven to work properly up to 2.43V analog supply.

Figure 10 shows the complete layout of the DAC, which occupies 0.38x0.28mm^2. The upper most part is dedicated to the digital circuitry (decoder, latency equalizer, and clock phase generation). Then, they come the level shifters, the latches, and the switch drivers. The central part is reserved for the switches and current source matrix. Here symmetry is maximally respected in order not to induce systematic mismatch [5]. The layout also includes the bandgap generator and reference buffers located at the bottom side.

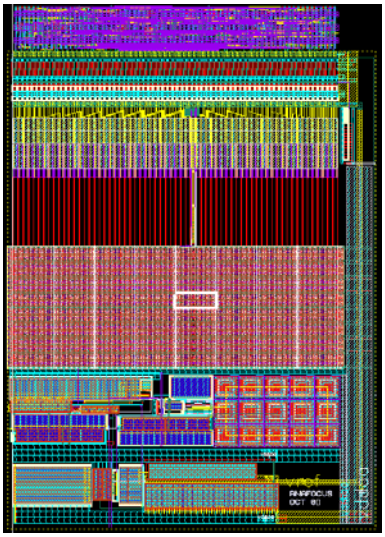

Figure 10 – DAC layout in 0.13um CMOS

Figure 11 shows the time-domain output voltage for a 2.32MHz input full-scale sinewave obtained from post-layout simulations. Corresponding spectrum is shown in Figure 12.

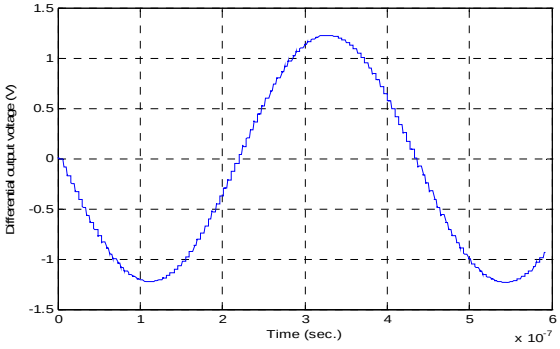

Figure 11 – Differential output for 2.3MHz input

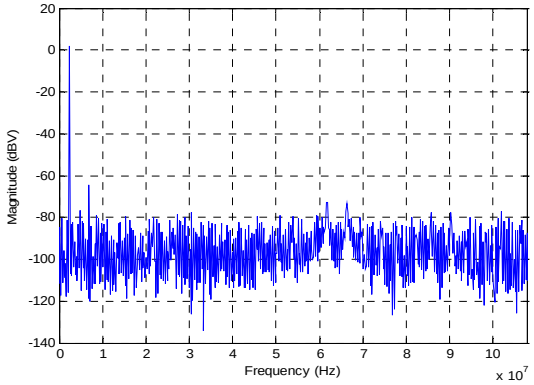

Figure 12 – Output spectrum for a 2.3MHz input sinewave

Figure 13 shows a histogram of the *SFDR* up to the third harmonic for a full-scale sinewave at 2.32MHz, in the presence of supply, temperature, corner variations and device mismatch. The worst-case *SFDR* is 55dBc.

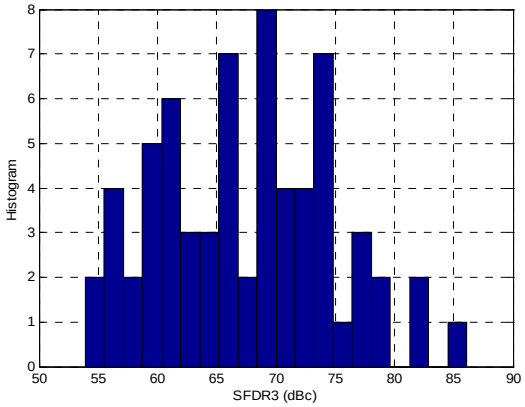

Figure 13 – Spreading of *SFDR* with temperature, supply, corners and device mismatch.

10. REFERENCES

[1] J.L. González and E. Alarcón: "Current-steering High-Speed D/A Converters for Communications," Chapter 3 in A. Rodríguez-Vázquez, F. Medeiro and E.Janssens (Editors): *CMOS Telecom Data Converters*, Kluwer Academic Publishers, 2003.

[2] Y. Cong and R.L. Geiger: "Switching sequence optimization for gradient error compensation in thermometer-decoded DAC arrays," IEEE Trans. on Circuits and Systems – II, Vol. 47 pp. 585-595, July 2000.

[3] G. A. M. Van der Plas, J. Vandenbussche, W. Sansen, M. S. J. Steyaert, and G. G. E. Gielen, "A 14-bit intrinsic accuracy Q2random walk CMOS DAC," *IEEE J. Solid-State Circ.*, Vol. 34, pp. 1708-1718, 1999.

[4] T. Chen and G.G.E. Gielen: "The analysis and improvement of a current-steering DACs dynamic SFDR-I: the cell-dependent delay differences," *IEEE Transactions on Circuits and Systems I,* Vol. 53, pp. 3-15. January 2005.

[5] M. Delgado-Restituto, et al: "An embedded 12-bit 80MS/s A/D/A interface for power-line communications in 0.13um pure digital CMOS technology," IEEE International Symposium on Circuits and Systems, pp. 4626-4629, 2005.