A LOW-COMPLEXITY DATA WEIGHTED AVERAGING (DWA) ALGORITHM IMPLEMENTATION

Ramón López-Holloway[*] *and Miguel García*

Instituto Nacional de Astrofísica Óptica y Electrónica,
Luis Enrique Erro No.1, Puebla, Mexico, C.P. 72840, Departamento de Electrónica.

holloway@inaoep.mx, mgarcia@inaoep.mx

ABSTRACT

A low-complexity digital control for implementing the Data Weighted Averaging (DWA) algorithm is presented. In order to verify the logical operation, transistor level simulations are performed with HSPICE. The 0.35µm standard CMOS technology is used for transistor level simulations.

1. INTRODUCTION

Dynamic Element Matching (DEM) and Error Shaping have become very important linearization techniques in high resolution DACs and multibit Sigma-Delta modulators [1][2]. The DEM schemes are implemented with unitary elements steering DACs. The way the elements are selected gives the name to the algorithm, and this result in a given characteristic of dynamic matching. Some of the most important are: Individual Level Averaging (ILA), Clocked Averaging (CLA), Random Averaging, and Data Weighted Averaging (DWA) [1][2][3][4]. One of the simplest DEM scheme is the Data Weighted Averaging (DWA) [3] which selects the unitary elements cyclically. The main characteristic of the DWA is the capability to shape the spectrum of the mismatch error as a first order high-pass filter [3][5]. Although the concept of selecting the elements of the DWA is not complex; just a few papers explain the way it was implemented. The most common used approaches are the carrousel [6] and the barrel shifter [1]. Other works mention that a state machine is used. The main drawback of the carrousel method is that every stage must wait for the previous stage to settle, thus speed is limited. On the other hand, complexity of a barrel shifter increases exponentially with the numbers of inputs. An approach to implement the DAW algorithm with good compromise among speed, area, and complexity is presented in this paper.
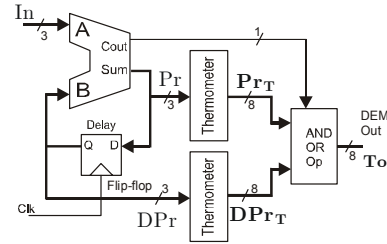

Figure 1. Block Diagram of the digital implementation of the DWA DEM.

In	Pr	Dpr
2	2	0
4	6	2
6	4	6

Figure 2. Sequence for In, Pr, and DPr

2. DIGITAL CONTROL IMPLEMENTATION

The proposed digital system to implement the DWA DEM is presented in Fig. 1. It is very similar to the barrel shifting approach [1], i.e., a full adder, a sum data, and delayed pointers are used. However, in our approach the barrel shifter or carrousel are replaced by a simple logic AND/Or operation block.

In order to explain the logical operation, a signal level analysis is presented. The data of the pointer (Pr) is the sum of the delay pointer (Dpr) and the input (In) sequence. Pr, DPr and In must be coded as positive binary integers. In this case 3 bits are used. Assuming an input data sequence of 2, 4, and 6, with 0 as the initial condition of the DPr, the sequence for Pr and Dpr is shown in Fig 2. The output sequence is better understood analyzing for the case In=4. Since the last data is 2, then

		T7	T6	T5	T4	T3	T2	T1	T0
Dprt	2	0	0	0	0	0	1	1	1
Prt	6	0	1	1	1	1	1	1	1

(a)

		T7	T6	T5	T4	T3	T2	T1	T0
$\overline{\text{Dprt}}$	2	1	1	1	1	1	0	0	0
Prt	6	0	1	1	1	1	1	1	1
AND		0	1	1	1	1	0	0	0

(b)

		T7	T6	T5	T4	T3	T2	T1	T0
$\overline{\text{Dprt}}$	0	1	1	1	1	1	1	1	0
Prt	2	0	0	0	0	0	1	1	1
AND		0	0	0	0	0	1	1	0

(c)

Figure 3. Logical Analysis for thermometer coded pointers. a) *In*=4, *Dpr*=2.b) Inverting *DPrt*. c) In=2, *DPr*=0

DPr=2 and Pr=6. Pr and DPr are coded to thermometer code (**Pr$_T$**, **DPr$_T$**), see Fig. 3(a). It can be seen that if **DPr$_T$** is inverted, and bitwise ANDed to **Pr$_T$**, the result is that *T6*, *T5*, *T4*, and *T3* are "1", and the rest are "0", see Fig 3(b). If the same analysis is done for the case In=2, Fig. 3(c), then *T1* and *T2* are "1", and the rest are "0", which represents the output sequence of the DWA DEM. It is necessary to point out that for this case the thermometer is coded from *T0* to *T7*, which represents 8 elements. In a normal 3-bits-to-thermometer code the outputs are coded from *T1* to *T7*. This is because a 3-bits full adder is used, and the sequence for "000" must be decoded. Thus, the full adder performs the modulo-8 operation between In and Dpr. As a result the output sequence is shifted by 1, but this does not divert the signal processing of the DEM. For the case In=6 and Dpr=6, then Pr should be 12, but the results is Pr=4 due to maximum count is 8, then the carry is 1 and the operation *6 Mod8 6 = 4* is performed. Again, Pr and Dpr are coded to thermometer code and **Dpr$_T$** is inverted, see Fig 4. For this case the output is obtained with the logical bitwise Or operation between **Pr$_T$** and **DPr$_T$**. Thus, the logical equation of the above operations is

$$T_i = (\text{Pr}_i + \overline{\text{DPr}_i}) \cdot C_O + (\text{Pr}_i \cdot \overline{\text{DPr}_i}) \cdot \overline{C}_O \qquad (1)$$

The final output sequence for the previous data is shown in Fig. 5. This system was also implemented at level transistor using CMOS 0.35μm standard technology. Figure 6 shows the results obtained with HSPICE for In=5. The obtained time delay is 3.62nS.

		T7	T6	T5	T4	T3	T2	T1	T0
Dprt	6	0	1	1	1	1	1	1	1
Prt	4	0	0	0	1	1	1	1	1

(a)

		T7	T6	T5	T4	T3	T2	T1	T0
$\overline{\text{Dprt}}$	6	1	0	0	0	0	0	0	0
Prt	4	0	0	0	1	1	1	1	1
OR		1	0	0	1	1	1	1	1

(b)

Figure 4. Logical analysis for thermometer coded pointers. a) *In=6, DPr=4* .b) Inverting *DPr$_T$*.

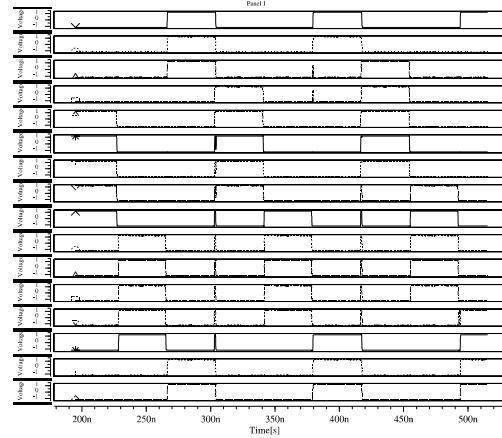| *In*	S7	S6	S5	S4	S3	S2	S1	S0
0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	1	1	0
4	0	1	1	1	1	0	0	0
6	1	0	0	0	1	1	1	1

Figure 5. Final output sequence

Figure 6. Simulation results with HSPICE. Input is held constant to In=5.

3. CONCLUSIONS

A low-complexity and efficient digital control for implementing the Data Weighted Averaging (DWA) algorithm has been proposed. This approach presents good trade off between speed and area. Simulation result presents a time delay of 3.62ns using 0.35μm standard CMOS technology.

4. REFERENCES

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