A DIGITAL TO ANALOG CONVERTER BASED ON A CHARGE PUMP CONCEPT

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1. ABSTRACT

A simple idea is presented in order to obtain an analog output signal for a given digital input. The circuit consists in two parts: an analog one (the charge pump) that allows to increase the analog output signal in a ΔV for each clock period until the output reaches the desired value, and a digital one, that controls the operation of the analog part.

2. THE ANALOG CELL

The circuit is presented in figure 1.

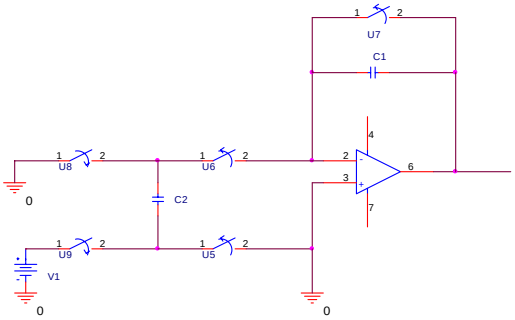

Figure 1. Basic charge pump cell.

The cycle begins with U8 and U9 closed. This assures that the reference voltage V1 charges C2 with Q2 = C2 V1. Once the capacitor voltage reaches a stable value, U8 and U9 opens and U5 and U6 closes, beginning the charge transference toward C1.
As the negative input of the opamp is connected to the virtual ground, the charge present in C2 will be injected to C1, leading to a ΔV voltage increment at the output. If this cycle is repeated 2^n times (the number of clock cycles necessary to reach the digital value for conversion), the analogue output voltage will reach to $2^n\Delta V$, which will be the corresponding converted analogue voltage of the digital input data.

This process is illustrated in figure 2. It can be noted that the slope of the analog output voltage can be adjusted by changing V1 (the reference voltage) or the C1/C2 capacitor ratio, but it is independent of the pulse width of the clock.

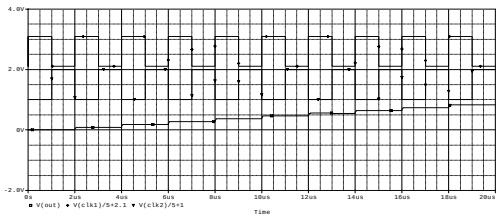

Figure 2. Simulation of the basic cell. Clocks and analog output.

The time maintaining the switches on should be large enough in order to allow the capacitor to be full charged. Due to this fact, the maximum working frequency can be calculated as:

$$f_{max} = \frac{1}{T_1 + T_2}$$

where T_1 and T_2 are the times to completely charge and discharge C2.
For this design, the total amount of time is around 300 ns, which gives a maximum possible frequency of 3.33 MHz.
This time can be reduced but this aspect presents an obvious limitation. For an 8 bits converter, the total amount of conversion time in the worst case condition (Digital data = FF) is 256 * 300 = 76.8 us.
This presents another limitation that is the variable conversion time, depending on the digital input.
Despite those undesirable characteristics, the circuit only need for working a reduced digital control part leading to a very cheap device in terms of area and design effort.
The digital control part is shown in figure 3.

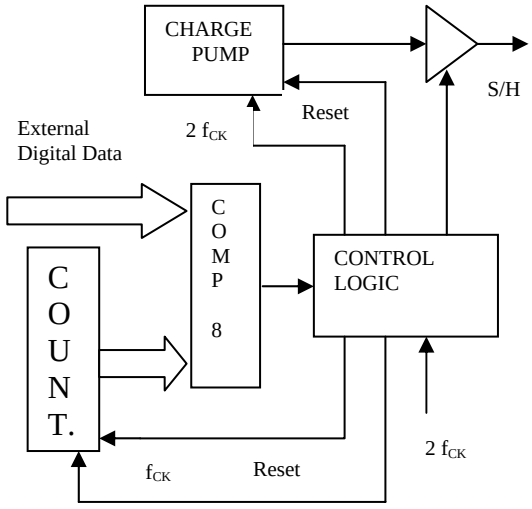

Figure 3. Block diagram of the control logic

As it can be seen in figure 3, the schematic is very simple. The S&H block is added in order to deliver a steady signal in between samples. This circuit performs the following operation: at the beginning of the conversion cycle the digital data to be converted is presented in the input and the n bits counter and the charge pump are reset. When the cycle starts, 2^{n+1} cycles of the main clock will pass until the output analog signal reaches the correct value (marked as 2*fck in the block

diagram of figure 3), while 2^n cycles of the fck will ensure the analog output to reach the desired value.

The slope of the analog output and thus the maximum attended output voltage can be changed. For design purposes, the following relationship can be applied

$$Vout\_máx = 2^n . \frac{C_2 V_{ref}}{C_1}$$

As can be seen, for a fixed resolution (n bits) the slope can be changed by moving the capacitance ratio or the reference voltage. This gives two freedom degrees in order to adjust the full scale range.

3. NON IDEALITIES

Main sources of errors in the output voltage are:

- the charge injection due to clock feed-through owing to the parasitic capacitances of the switches plus the charge injection of the switches themselves when they are turned off.
- The operational amplifier used in the circuit. This introduces ringing in the ladder step due to settling time, beside the proper non idealities of the opamp (offset, finite gain, finite input impedance, etc.)
- The capacitors ratio. It has been proven by simulation that the parasitic capacitors have more relevance when C1 and C2 are small. This can be solved by making them bigger enough.

4. LAYOUT AND RE-SIMULATION

The Layout is shown in figure 4. The circuit was designed and simulated using the 1.6u AMIS technology.

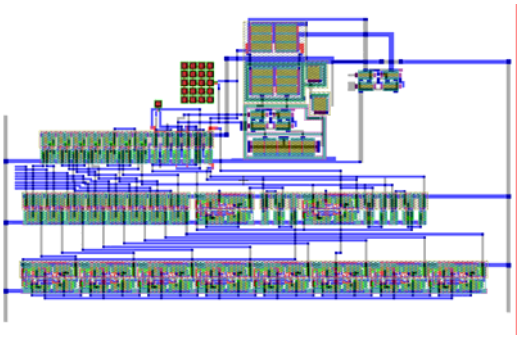

Figure 4. A layout of the circuit, including the control part.

The size is approximately 0.5 mm^2 (1x0.5) and the largest part is obviously the digital one, which was made using standard cells. The design was extracted and re-simulated and the results are shown in figure 5.
It can be observed three curves: The upper shows the analog output of the DA converter. At the end of the conversion (Sample & Hold signal is high) the analog output is held in an analog memory point, and then the system is reset (the output reset signal, in the middle of the graphic), allowing the converter to start a new conversion cycle.

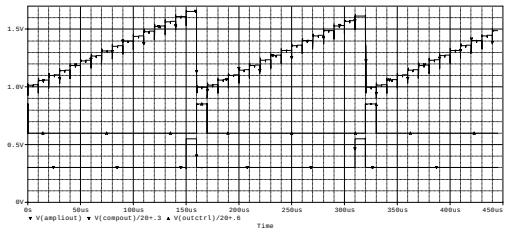

Figure 5. a) analog output. b) Output control reset. c) S&H control

The whole system is completely stand-alone and the master clock signal (not shown in simulation) is set to 100 Khz.

5. CONCLUSIONS

A simple idea was shown. It was proved that it works, it is feasible and, of course, it is usefull for implementations where the speed is not a critical issue. It should be noted that the same principle could be used in the implementation of other converters, even A to D converters. For example the single or double ramp AD converter, using the charge pump principle for generating the ramp.
Some non idealities have been depicted, showing that the circuit is far to be perfect. Beside of this fact, the simplicity of the idea and its implementation (almost automatic, using standard cells) are attractive features and offers some good reasons to use it in the cases where the constraints are not very hard.

6. REFERENCES

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