# AN RF-CMOS LNA AND MIXER MERGED DESIGN STRATEGY

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## ABSTRACT

Low Noise Amplifier and Mixer design considerations for 2.45 GHz Bluetooth applications have been studied. A detailed noise analysis is presented. A design strategy for an inductively degenerated common-source LNA with cascode transistor and current-commutating Mixer is proposed, considering the tradeoffs between noise, linearity, power consumption and matching of impedances. Additionally, this work presents a new expression to estimate the LNA noise figure considering the noise introduced by the transconductance stage and the cascode device. A 2.45 GHz LNA-Mixer has been designed and simulated in a $0.35\mu m$ $4M2P$ CMOS technology to validate the proposed strategy. Some performance results obtained through simulations are: $NF$=$7.9dB$, Voltage Gain=$27dB$, $P_{IIP3}$=$-14.4dBm$, $IF = 1MHz$ and power consumption of $15.6mW$ at $3.3V$ power supply.

## 1. INTRODUCTION

LNA and Mixer are key components in a wireless receiver. Its performance affects subsequent blocks requirements. Also, tradeoffs between LNA and mixer decrease front-end performance if they are designed independently. However, many works have been presented for the LNA and mixer disjunct designs decreasing possibilities to getting most desirable front-end. This work presents a strategy to design a LNA and a mixer conjunctly. Therefore, guidelines from literature to design independent blocks were adapted. Additionally, tradeoffs between enough gain, low noise figure, high linearity, stable input impedance and ports isolation with low power consumption for portable applications are considered in order to establish a new design strategy.

Sections 2 and 3 explain the considerations and strategy used in CMOS LNA-Mixer design. Also, some LNA design strategies presented in literature consider only the noise introduced by the transconductance stage and neglect the cascode device noise contribution; nevertheless, this work proposes a new theoretical expression to explain that the cascode device can degrade significantly the LNA noise performance, depending on the biasing conditions and device dimensions. As an example, a 2.45GHz LNA-Mixer is designed in a $0.35\mu m$ $4M2P$ CMOS technology, and its simulation results are presented in section 4. Finally, conclusions are shown in section 5.

## 2. LNA AND MIXER JOIN DESIGN CONSIDERATIONS

In order to present the design considerations it is mandatory to review the standard specifications before discuss each consideration. Furthermore, design considerations must establish the used architecture and technology.

Circuits used to validate the design strategy were implemented and simulated using a $0.35\mu m$ CMOS. This technology is well suited and widely used in literature in a RF receiver stage for Bluetooth applications at $2.45\ GHz$. In agreement with the literature inductively degenerated common-source (CS) LNA with cascode transistor and current-commutating mixer are well-fitted architectures to accomplish an LNA-Mixer join design.

According to the results presented in literature [1]–[3] and circuit analysis made for inductively degenerated common-source LNA with a cascode transistor and current-commutating Mixer, shown in figure 1 and 2, the following considerations must be attained by designing a CMOS LNA and Mixer:

**a)** A great commitment between impedance matching, gain, low noise and linearity. The LNA transconductance stage must be matched at the input in the desired frequency band. The gain of the transconductance stage depends directly on the current unity gain frequency $\omega_T$. On the other hand, the noise figure is reduced as $\omega_T$ increases. Thus, the transistor channel length $L$ is chosen to be as small as possible to increment $\omega_T$.

**b)** Third order intermodulation ($IM3$) of the transconductance stage, can be reduced not only by adjusting the out-of-band terminations but also for a good bias point (equation (1)). In this way, interactions between third order coefficient $g_3$ and second coefficient $g_2$ (equation (2)), which relate drain current to gate-source effective voltage, are reduced [2], [3]. Being $\omega_0$ the resonance central frequency, $R_s$ is the antenna output resistance, $g_1$=$g_{m1}$ and $L_s$ the degenerating inductance.

$$P_{IIP3} \approx \frac{4}{3}\left(\frac{\omega_0}{\omega_T}\right)^2 \frac{R_s^2}{g_1}\frac{1}{|r_3'(\Delta\omega, 2\omega_0)|} \quad (1)$$

$$r_3'(\Delta\omega, 2\omega_0) \approx \frac{g_3}{g_1^4} - \frac{2g_2}{3g_1^4}\left\{\frac{2\omega_0 L_s}{4\omega_0 C_{gs1}R_s + j3}\right\} \quad (2)$$

**c)** On the assumption that LNA input is conjugately matched, the noise factor of the transconductance

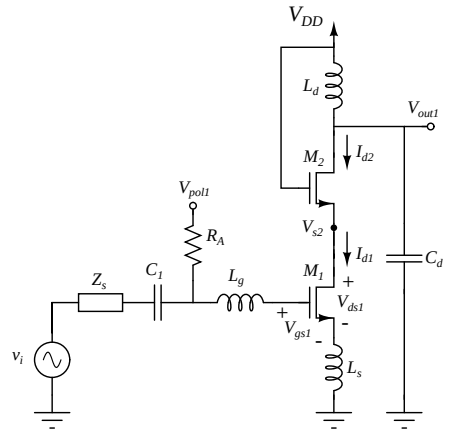



Fig. 1. Inductively degenerated CS LNA with cascode transistor.

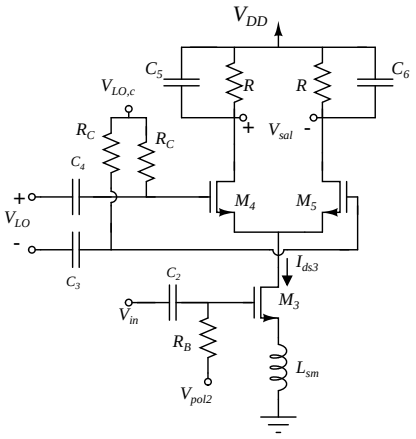



Fig. 2. Single-balanced current-commutating CMOS mixer.

stage can be approximated as follows:

$$F_{Transc} \approx 1 + \frac{w_0}{w_{T1}}\gamma_1 w_0 C_{gs1} R_s \left\{ \frac{1}{\alpha_1} + \frac{\delta_1 \alpha_1}{5\gamma_1}\left(1 + \frac{1}{(w_0 C_{gs1} R_s)^2}\right) - 0.79\sqrt{\frac{\delta_1}{5\gamma_1}} \right\} \quad (3)$$

where $\gamma_1$ and $\delta_1$ are bias dependent noise parameters, $w_{T1} \approx g_{m1}/C_{gs1}$, $\alpha_1 = g_{m1}/g_{d01}$ and $g_{d01}$ is the gate-drain conductance in triode region, for the same $V_{GS1}$ and zero $V_{DS1}$.

Similarly, a cascode noise factor with regard to the noise introduced by the LNA input source, can be approximated as follows:

$$F_{cascode} \approx 1 + \frac{4\omega_0^4 R_s \gamma_2}{\omega_{T1}^2}\frac{C_{gs2}^2}{g_{m2}}\left\{ \frac{\alpha_2 \delta_2}{5\gamma_2} + \frac{(1 + \frac{C_p}{C_{gs2}})^2}{\alpha_2} - 0.79\left(1 + \frac{C_p}{C_{gs2}}\right)\sqrt{\frac{\alpha_2}{5\gamma_2}} \right\} \quad (4)$$

where $C_p$ is total capacitance in the node $V_{s2}$ (without $C_{gs2}$), and $g_{m2}$ is $M_2{}'s$ transconductance. Therefore, if $\omega_{T1}$ is specified, there is a optimal quality factor $Q_{in,opt}$, and a optimal width ($W_{1,opt}$), so that the transconductance's noise factor ($F_{Transc}$) is minimized.

Provided that, if the contribution to the LNA total noise factor ($F_{total}$) from the cascode device is insignificant, $F_{total}$ can be decreased by selecting $W_1 = W_{1,opt}$. Moreover, if cascode noise at the interest frequency can not be neglected, it is necessary to take both transconductance and cascode noise factors into consideration. Simultaneously, it's necessary to have special care in the design and selection process of the inductors in order to avoid low quality factors.

**d)** The $M_2{}'s$ width selection for the cascode device, establish a top voltage value for the gate-source of $M_1$. The goal is keeping $M_1$ in active region. Additionally, for different $W_2/W_1$ relations and bias points there is $W_{1,opt}{}'s$ different values to get a good noise performance.

**e)** Output signal to noise ratio including flicker noise ($SNR_{out}$) generated in the switching pair by direct mechanism [4], increases with local oscillator amplitude ($A_{LO}$). Also $SNR_{out}$, increases with switching pair transistors gate area and with ($V_{gs3} - V_t$) and $C_{gs3}$ values decreasing. Nevertheless, scaling down the effective voltage ($V_{gs3} - V_t$) noise figure increases due to transconductance thermal noise and reduces the mixer's signal to noise ratio.

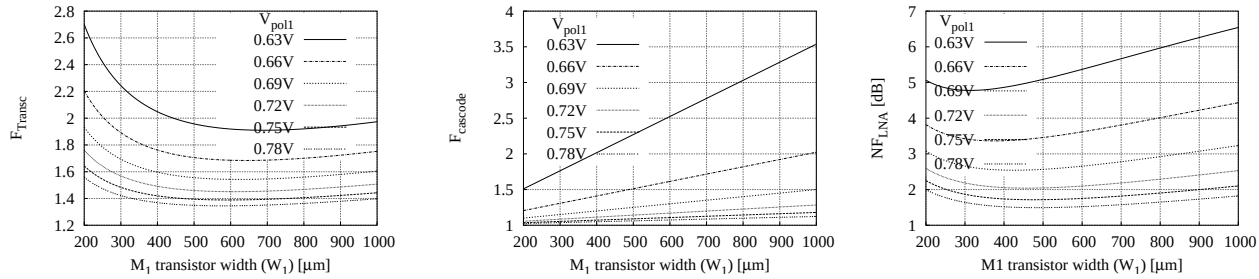
**f)** Moreover, thermal and flicker noise performance of switching pair get improved by increasing local oscillator amplitude. However, according to the results shown in [3], an optimal amplitude value in high frequency exists after which intermodulation increases.

## 3. LNA AND MIXER JOIN DESIGN STRATEGY

This section shows the basic steps which allow to obtain fundamentals tradeoffs between the LNA and the Mixer noise, linearity, impedance matching, power consumption, gain and ports isolation. Figure 3 indicates the design strategy developed based on the former sections. Notice that bias voltage, transistor dimensions and coil values are used as design variables.

We first define the LNA-Mixer Bluetooth specifications. Next, we choose the minimal allowed channel length in order to increase the gain and to improve the noise performance. We further establish the widths relations between the cascode and the transconductance transistors, $W_2$ and $W_1$ (in this design $W_2/W_1 \approx 2/5$). The main goal is to insurance that at maximal bias tension, $M_2$ and $M_1$ stay in the saturated region. Following, the cascode and transconductance noise factors are estimated. Figure 4 presents each of these results and the LNA total noise figure. The transconductance stage bias voltage ($V_{pol1}$) and the transistor widths were chosen as independent variables for this analysis.

At this point, it is evident that noise factor at different $M_1$ bias voltage ($V_{pol1}$) is greater for the cascode device than for the transconductance stage (see figure 4). Therefore, $W_1{}'s$ value for the LNA best noise performance is different than $W_1{}'s$ value for the minimal point of transconductance noise factor. Under these considerations, a value range of $W_1$ exists for which it improves the LNA noise performance, for different bias $V_{pol1}$ values and for a pre-established $W_2/W_1$ relation (in this




(a) (b) (c)

Fig. 4. (a) LNA transconductance stage noise factor; (b) Cascode transistor noise factor; (c) LNA total noise factor.

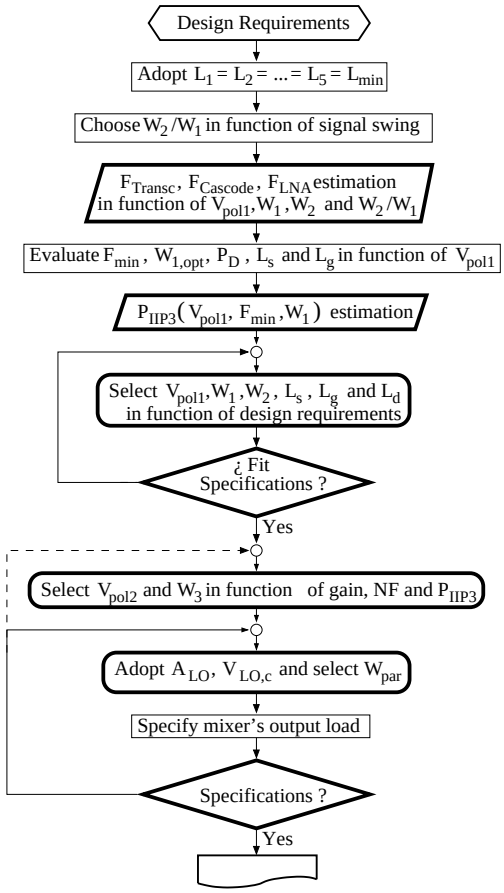



Fig. 3. LNA and Mixer Design Strategy.

case $W_2/W_1 \approx 2/5$). Therefore, for each value of $V_{pol1}$ was found a width of $M_1$ ($W_1$) for which the LNA noise figure is minimized.

In addition, for each channel width ($W_1$) was made an estimation of power consumption and the third-order input intercept point $P_{IIP3}$ through (1). A polarization voltage $V_{pol1}$, $L_s$ and $L_g$ values, and transistors width ($W_1$ and $W_2$) were selected based on power consumption, noise, linearity and input impedance requirements. Besides, to obtain a narrow band LNA was used a resonant parallel LC circuit connected in the drain of $M_2$ to increase the gain in the wished frequency band. So, $W_1$=460$\mu m$, $W_2$=180$\mu m$, $V_{pol1}$=0.73$V$, $L_s$=0.3$nH$, $L_g$=5.7$nH$ and $L_d$=5$nH$ were selected.

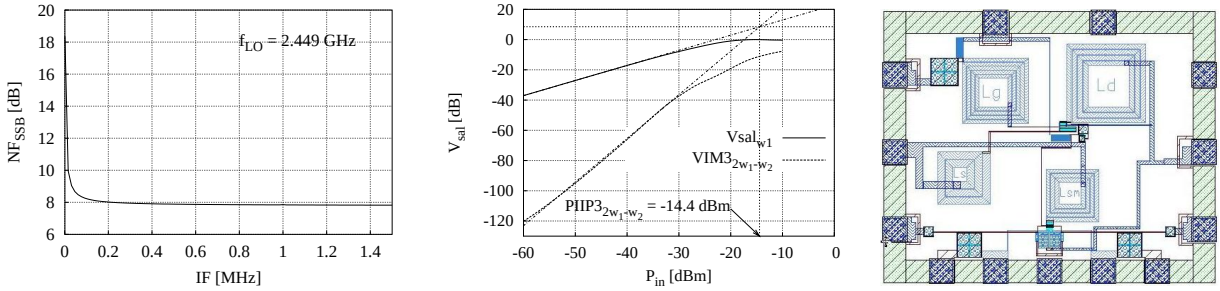
Given these values, we looked for inductor's quality factor that accomplish noise, bandwidth and gain performance. In this process, we used an optimization tool from ASITIC [5] to find the higher quality factor for an specific area. By simulation results, we found that the inductor's least quality factor must be greater than 2.5 in order to obtain an LNA's noise figure lower than $5dB$. For the specific cases where the designed inductors didn't accomplish with the required performance, the area restriction was modified in ASITIC.

On the other hand, mixer's transconductance stage design depends of LNA output impedance. If $|Z_{Cgs3}|>|Z_{Lsm}|$, increasing the size of $M_3$ transistor the gain of the tranconductance stage rises, due $|Z_{Cgs3}|$ is decreased (equation (5)). Besides, increasing the width of $M_3$ transistor reduces the mixer equivalent input impedance, and consequently, it diminishes the LNA gain, due to the fact that equivalent impedance connected in drain of $M_2$ decreases. In consequence, there exists a value of $W_3$ for which it is obtained a maximum gain in the output of mixer transconductance stage.

$$G_{M3} \approx \left| \frac{i_{d3}}{v_{out1}} \right| \approx \frac{\omega_{T3}/\omega}{|\omega_{T3} Lsm + Z_{Lsm} + Z_{Cgs3}|} \quad (5)$$

Moreover, the bias voltage $V_{pol2}$ for $M_3$ was selected equal to the LNA transconductance stage bias point $V_{pol1}$ with the purpose of reducing bias points ($V_{pol2}$=$V_{pol1}$≈0.73 $V$), by the way given this bias point must guarantee all requirements. Degenerating inductor $L_{sm}$ was selected in such a way that Mixer linearity performance is suitable: to major inductance $L_{sm}$ value, linearity gets improved [3], but Mixer's transconductance stage gain reduces. By selecting transconductance stage bias point and $L_{sm}$ inductance, $W_3$ was used as a design variable to obtain a suitable coupling between *LNA* and Mixer. In this way, it obtains highest gain at transconductance stage output according to bias conditions.

However, before $W_3$ selection it is necessary to evaluate transconductance stage linearity performance. By increasing $M_3$ transistor width, the intermodulation point at transconductance stage input gets improved under specific considerations ($V_{pol2} = 0.73\ V,\ L_{sm} = 2.6\ nH$ and $W_3 > 100\mu m$).




(a) (b) (c)

Fig. 5. LNA and Mixer post-layout results: (a) Single-Sideband Noise Figure $NF_{SSB}$; (b) $P_{IIP3}$ with $f_{LO}$=2.449 $GHz$, $f_1$=2.451 $GHz$ and $f_2$=2.452 $GHz$; (c) Layout of LNA and Mixer circuits.

TABLE I
SUMMARY OF LNA-MIXER SIMULATION RESULTS.

| **Specifications** | **This work** | **[6]** | **[7]** |
|---|---|---|---|
| Supply voltage $[V]$ | 3.3 | 2.7 $V$ | 1.8 |
| Power consumption $[mW]$ | 15.6 | 21.6 | 6.5 |
| Noise Figure ($NF_{SSB}$) $[dB]$ | 7.9 | 3.4 | 13.9 |
| Voltage Gain $[dB]$ | 27 | 23 | 21.4 |
| $P_{IIP3}$ $[dBm]$ | $-14.4$ | $-3$ | $-10$ |
| $f_{RF}$ $[GHz]$ | 2.45 | 2.1 | 2.44 |
| $S_{11}$ $[dB]$ | $\leq -14$ | $\leq -30$ | $\leq -13$ |

Switching pair linearity performance was estimated by considering results from [3]. These results show existence of a range for switching pair dimensions which improve Mixer linearity for a drain current $M_3$ and a local oscillator voltage range. There were made simulations for different $W_4 = W_5 = W_{par}$ values in order to find design commitments between noise and linearity with regard to switching pair transistor width. In final design, used for validate the proposed strategy, it was found a $W_{par}{}'s$ values range from $100\mu m$ to $120\mu m$. Consequently, $W_4$=$W_5$=$110\mu m$, $W_3$=$220\mu m$, $A_{LO}$=$1V_p$, $V_{LO,c}$=$1.5V$ were selected.

## 4. LNA AND MIXER POST-LAYOUT SIMULATION RESULTS

A $2.45GHz$ LNA-Mixer has been designed and simulated on a $0.35\mu m$ $4M2P$ CMOS technology in order to validate the proposed strategy. Figure 5(c) shows the LNA and Mixer layout accomplish through IC Station of Mentor Graphics. This layout obeys to $0.35\mu m$ CMOS C35B4C3 design rules of AMS. The final die area was $1mm^2$ including pads; despite, on-chip integrated inductors occupy a die area of $50\%$.

Table I and figure 5 present some of the LNA and Mixer performance specifications obtained through simulation in Eldo-RF and HSpice with foundry noise parameters in BSIM3V3 RF models. The inductors were simulated through the PI models extracted of ASITIC in the design process. Intermodulation tests were made with two tones at frequencies of $f_1$=$2.45GHz$ and $f_2$=$2.452GHz$, and a local oscillator frequency of $f_{LO}$=$2.449GHz$. In addition, table I presents performance specifications about other works [6], [7]. Based on these results, it deduces that LNA and Mixer design presents a better performance in relation to gain voltage, but linearity performance is lower than the presented in [6], [7]. The noise figure is higher than in [6], but [6] uses off-chip matching network. In our design, on-chip integrated inductors degrade significantly the noise performance.

## 5. CONCLUSION

The LNA-Mixer join design strategy was adapted from the literature guidelines. An LNA-Mixer was designed in a $0.35\mu m$ *CMOS* to validate the design strategy which takes into account the LNA and the mixer blocks matching. Simulation results show that Bluetooth standard requirements were accomplished. The noise and linearity expressions from literature for inductively degenerated common-source LNA with cascode transistor and current-commutating mixer were reviewed and new expressions were formulated. The proposed design strategy considers noise, linearity, gain, power consumption, matching of impedances and ports isolation tradeoffs using the device dimensions and bias as design variables. The circuit was sent to fabrication, however, at the time that this paper was submit for this workshop the circuit have not been returned yet.

## 6. REFERENCES


[1] D. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, 1997.

[2] E. Roa, J. Navarro, and W. Noije, "A Methodology for CMOS Low Noise Amplifier Design," in *16th Symposium on Integrated Circuits and Systems Design. IEEE Computer press*, 2003, pp. 14–19.

[3] E. Terrovitis, "Analysis and Design of Current-Commutating CMOS Mixers," Ph.D. dissertation, University of California, Berkeley, 2001.

[4] H. Darabi and A. A. Abidi, "Noise in RF-CMOS Mixers: A Simple Physical Model," in *IEEE J. Solid-State Circuits*, vol. 35, no. 1, 2000, pp. 15–25.

[5] (2005) Asitic documentation. [Internet]. Visite: http://rfic.eecs.berkeley.edu/ niknejad/asitic/asitic.html

[6] H. Sjöland, A. Karimi-Sanjaani, and A. A. Abidi, "A Merged CMOS LNA and Mixer For A WCDMA Receiver," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1045–1050, 2003.

[7] F. Beffa *et al.*, "A 6.5-mW Receiver Front-End for Bluetooth in 0.18-$\mu m$ CMOS," in *IEEE MTT-S Int. Dig.*, vol. 1, San Diego, CA, Jun. 2002, pp. 501–504.