LOW-POWER CONTROLLER FOR SENSOR NETWORKS

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ABSTRACT

In this paper, synthesizable low power microcontroller core is proposed for Wireless Sensor Network (WSN) application. The core performs full set of MSP430 arithmetic operations and merged compare-skip instruction. To generate dense code, the instruction set architecture (ISA) adapted register-memory architecture and multi-cycle datapath is implemented. The circuit is synthesized using 0.18-μm standard CMOS process to evaluate power estimation. Synthesized result shows low current consumption and gate count with barrel shifter. The power estimation shows 3.75pJ/bit per register-register instruction.

1. INTRODUCTION

Low-voltage and low-power 8-b, 16-bit, 32-bit micro processors are required for portable products and wireless sensor networks (WSN). In the market, conventional architectures such as PIC16/24, AVR, and ARM dominate consumer electronics and prototype WSN applications [1][2][3]. By using an advanced circuit techniques and low-voltage silicon technology, their power consumption is controlled enough to be used in typical hand-held application. However, wireless sensor networks are ideally suited for long-lived applications deployed at large densities for low cost. Unfortunately, the current WSN platforms built from commercial off-the-shelf (COTS) components have a lifetime of no more than two years [4][5]. This paper reports the design result of a low-power and synthesizable microprocessor to extend lifetime of sensor networks. Since the static power consumption is dependent on circuit size, instruction set is specially designed to reduce circuit size taking account I/O-bound characteristic of sensor network application and commercial embedded controller chip. As a result of the work, synthesis results and power estimation (calculated by static power analysis) is presented in final section.

2. 16-B LOW POWER CONTROLLER

2.1. Sensor network applications

The sensor nodes perform sensing-encapsulating-radio-sleep cycle and the program is I/O bounded definitely.

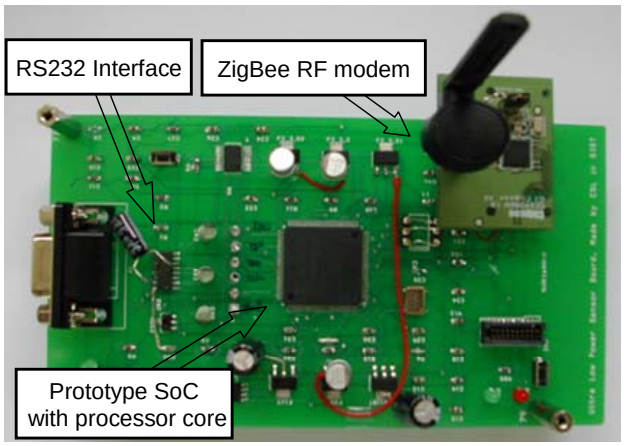


Fig.1. Prototype SoC implemented in FPGA.

And conventional sensor network platform adopted AVR core and MSP430 core [4][6] that shows low power consumption and high performance for high level language programs. The commercial controller chips are equipped very small memory providing optimization opportunity on instruction word.

2.2. Instruction set architecture

Instruction set architecture is designed to reduce instruction memory size and make machine to achieve CPI=1. The operation covers common arithmetic instructions of commercial microcontrollers and also includes barrel shifting, decrement/increment and skip if zero instruction to accelerate loop. Address offset and abstract address immediate are limited under 16bit while the datapath is 16bit wide since memory requirement does not need wide address space.

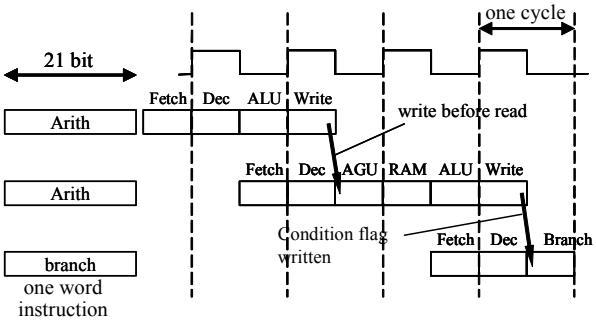
2.3. Two-stage pipeline

Proposed design consists of 2 stages: decode/ALU and register file/data memory. The register file and data memory plays pipeline register to minimize pipeline overhead that have severe static power consumption.

3. SYNTHESIS RESULT

3.1. FPGA prototype for verification

Fig.1 shows an FPGA prototype that includes GPIO, UART, SPI and other auxiliary logics. In a PCB for



* Fetch next instruction address calculation
* AGU access address resolution
* RAM memory access time
* Write write-back to register, flag or memory

Fig.2. Two stage pipeline and multi-cycle control.

TABLE I
COMPARIZON OF SYNTHESIS RESULT AND POWER ESTIMATION

Quantity	MSP430 compatible	Proposed architecture
Energy per instruction(minimum)	170pJ	60pJ
Energy per instruction(maximum)	700pJ	142pJ
Static power consumption	98nW	40nW
Gate count	6825	3405
Maximum operating frequency	58Mhz	57Mhz

Commercial MSP430 product energy consumption was 148pJ/V/instruction [7] and compatible processor marked 55~216pJ/V/instruction

demonstration, RF modem, RS232 line driver and FPGA configuration flash is embedded to show operation of proposed design.

3.2. Speed and area

Proposed design is implemented using 0.18-µm standard silicon process to evaluate power performance. The resulted circuit size is about 3500 gate count and the maximum operating frequency is 57 MHz.

3.2. Power estimation

Static power analysis is performed to evaluate energy consumptions per instructions. An MSP430 cycle-level compatible processor is implemented on same silicon process to be used for comparison. The proposed architecture outperforms MSP430 compatible processor taking advantage of CPI=1, multiple bus that reduces transition rate and small circuit size.

4. CONCLUSION AND FUTURE DIRECTIONS

To satisfy increasing demand of today's evolving wireless sensor networks, embedded controller must be low-power without degradation of performance. In this paper, a synthesizable 16-bit microprocessor is reported. The architecture covers all arithmetic and logical instructions and also includes increment/decrement with compare. Harvard memory model and 2-stage pipeline is used to increase performance and multi-cycle control is adopted for dense code. Total register file size and memory address offset for indexed access mode is limited to maintain circuit size and achieve high code

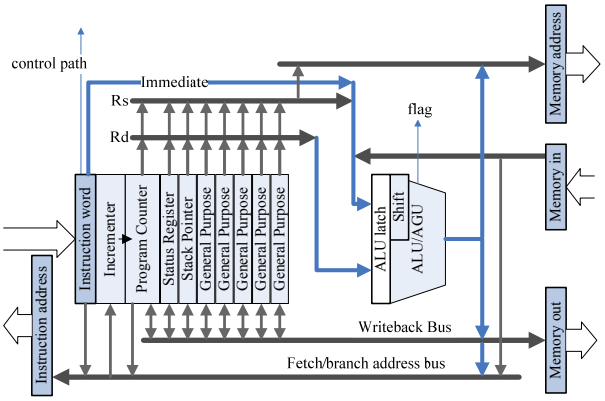


Fig.3. Diagram of datapath. To reduce bus activity and CPI, numbers of buses are used.

density. The HDL description is synthesized using 0.18µm standard CMOS process to evaluate power consumption and performance. The circuit size is 3405 gate count and maximum operating frequency is 57 MHz including memory subsystem. The energy consumption per instruction marked 3.75pJ/bit. This project is currently in performance evaluation phase for the program coded by high level language. Considering this result, a revised version of instruction set architecture will be designed.

5. REFERENCES

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