Design Models Based on Experimental Data for VCOs Including Temperature Effects

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ABSTRACT

In order to verify the circuit performance deduced from spice results, experimental data of Current-Starved (7-, 9- and 11-stage) and Schmitt Trigger VCOs are presented. From these results and assuming identical work conditions the Schmitt Trigger VCO presented the lower oscillation frequency f_0 at a control voltage $V_{ctrl,0}=½V_{DD}$. In that sense, the relative error between simulation results and experimental data was that of the Schmitt Trigger response (7.4%) at room temperature. In order to fit the frequency-voltage characteristic of VCOs an analytical model based on a gaussian approach is proposed. Using this model an estimation of the VCOs' performance to temperatures higher than room temperature indicates that the lowest sensitivity is presented by the Schmitt Trigger circuit, -1.8 kHz/°C, at $V_{ctrl}= V_{DD}$.

1. INTRODUCTION

It is well known that oscillator circuits are basic building blocks in several fields of applications. One of them is that for measuring technologic parameters, from which the delay τ_d is the typical one to describe the dynamic of digital circuits. Another use case is as a clock generator, where circuit's activity under the control of a clock is usually mandatory. According to that the control of the clock frequency is as important as the duty cycle of the signal, thus the simple clock generator is not always the best option design because the oscillation frequency f_{osc} is not under the designer's control. On the other hand, since the frequency is a function of the current I_{BIAS}, several voltage controlled oscillators (VCOs) have been proposed. A couple of them, current-starved and Schmitt Trigger, were analyzed in [**1**] for evaluating their frequency-voltage characteristics. Now, in this paper experimental data of both Current-Starved and Schmitt Trigger VCOs are presented. Also, in order to reduce influences acting together with measured values an automatic test environment (ATE) has been developed. The frequency-voltage characteristic of VCOs is presented in section 2, where room temperature (T_0) and higher have been taken into account in order to evaluate the VCOs' performance. Math design models deduced from experimental data are proposed in section 3. From these models an extension of the VCOs' performance at higher temperatures is discussed in section 4. Finally, in section 5 conclusions of this work are given.

2. EXPERIMENTAL RESULTS

In order to minimize as much as possible influences acting together with measured values an automatic test environment (ATE) based on a commercial PSoC has been developed. Using this development we expect correct systematic influences by running routines that establish well-defined test methodologies. On the other hand, since the ATE allows acquire/store data for post processing, from experimental data is possible verify simulation results, enhance lumped design models, and estimate the circuit performance under severe work conditions as well.

2.1 ATE Development

The ATE provides quality results by optimizing both internal/external resources and communication protocols. External resources are commercial ICs for generating/measuring electrical signals, to establish suitable test algorithms, and also for defining communication links between internal/external resources and the device under test (DUT). In practice, the 24 MHz-CY8C29466 PSoC offers us take advantage of both its converters' resolution and their respective conversion rate. Thus, it is possible to configure the resolution of analog-to-digital (A/D) and digital-to-analog (D/A) converters from 6- to 14-b, and from 6- to 9-b, respectively [**2**]. D/A converters can been configured to implement up to 4 incremental voltage sources, and just one 12-b A/D converter is required to measure up to 8 voltage nodes by adding the CD74HC4051 analog multiplexer [**3**]. Lab equipment can be used to measure these parameters by developing master-slave architectures. In that sense, the ATE includes Agilent Instruments (54622D Mixed Signal Oscilloscope, 4192A Impedance Analyzer) mainly for testing to higher than the PSoC`s capabilities.

2.2 Experimental Data at $T=T_0$

Using design models reported in [**1**] Current-Starved and Schmitt Trigger VCOs where designed with help of design rules of a 1.5µm CMOS fabrication process. Fig 1a shows experimental results of 7-, 9-, and 11-stage Current-Starved oscillators as function of the control voltage V_{ctrl}. Transistors of the basic delay-stage was sized in order to obtain a frequency of the order of 263.3-, 204.8-, and 167.6-kHz for 7-, 9, and 11-stage VCO, respectively, all of them at $V_{ctrl,0}=½V_{DD}$. From

experimental results a voltage $V_{ctrl,0}$=2.59V is obtained for V_{DD}=5V, i.e. a relative error $\delta_{(M)}$=3.47% was calculated.

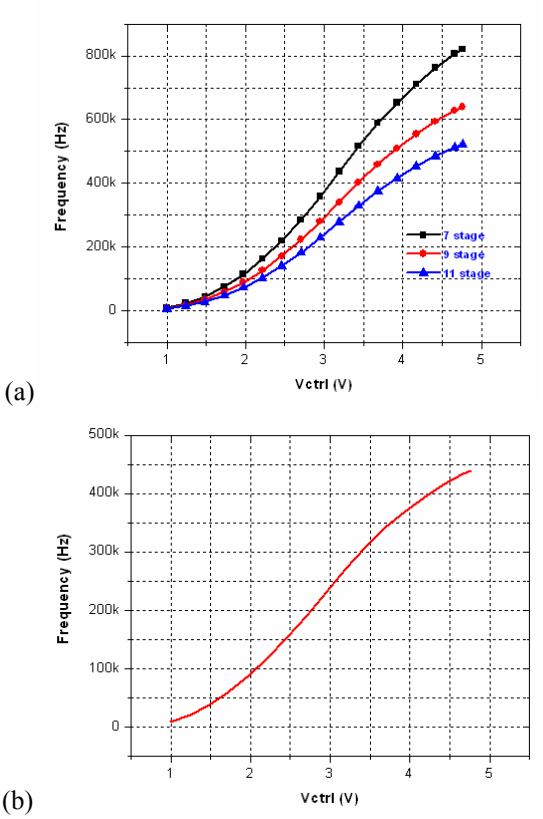


Fig. 1 Experimental response of VCOs at room temperature (T_0=27 °C). Current-Starved (a) and Schmitt Trigger (b).

Since the basic model is focused to obtain a frequency f_{osc} as function of several parameters under the designer's control, it was easy to obtain a linear model:

$$f_{osc} \approx 185.053\times10^{3}\cdot A\cdot\left(V_{ctrl}-1.687\right) \qquad (1)$$

where [$\mathbf{f_{osc}}$]=Hz, A=11/**n**, and **n**={7, 9, 11}is the number of stages. This result is limited by 2.2V≤V_{ctrl}≤4.2V, where a linear correlation coefficient **r**=0.999 was obtained. Also a Schmitt Trigger VCO has been tested. The response, shown in Fig. 1b, can be approximated into a linear region also limited by 2.2V≤V_{ctrl}≤4.2V:

$$f_{osc} \approx 144.47\times10^{3}\cdot\left(V_{ctrl}-1.365\right) \qquad (2)$$

where ***r***=0.997. Since the proposed frequency f_{osc} was 204.8kHz at $V_{ctrl,0}$=½V_{DD}, the relative error is $\delta_{(M)}$=10.0% because from experimental data $V_{ctrl,0}$=2.78V. However, considering $V_{ctrl,0}$=½V_{DD}, the relative error due to the measured frequency is (11.7%, 11.3% and 11.3%) and 24.9% for (7-, 9- and 11-stage) Current-Starved and Schmitt Trigger, respectively.

2.3 Experimental Data for T>T_0

In conjunction with the ATE a system with control of temperature (SCT) was developed to analyze the thermal influence on the frequency-voltage characteristics of VCOs. Fig. 2 depicts the SCT, where a thermal insulation (not shown in the figure) insulates the DUT from the ATE. The SCT includes both a thermometer and an open window (radii $\mathbf{r}_{TCS}$=2 in) by which a heater supplies a heat flow of air. Once temperature reaches stable values the DUT is powered, then the ATE's functions run in order to obtain a useful density of points with a measured time of a few seconds. An extension of responses shown in Fig. 1 is given in Fig. 3, where frequency-voltage characteristics for T=35, 40, and 45 °C have been included. It is well known that scattering effects increase as temperature increases too. That means a lower current density or equivalently a lower frequency response. The latter is because the carrier mobility follows the law $\sqrt{(T_0/T)^3}$, whereas the MOS threshold voltage variation is approximately 19mV/ºC [**4**]. The major frequency variation was observed at high gate voltages.

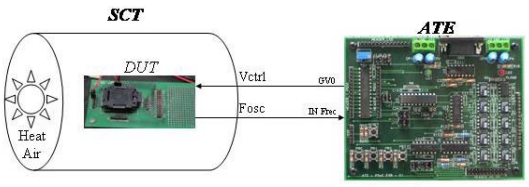


Fig. 2 Whole setup for measuring the VCOs' response under temperature variations.

In practice, because the gate voltage is actually a wide pulse signal that can be visualized as a quasi-continuous signal self-heating occurs affecting the frequency-voltage characteristic [**5**]. However, from experimental results is clear that the Schmitt Trigger oscillator presents lower frequency variation than Current-Starved designs.

3. DESIGN MODELS

From the mathematical point-of-view a gaussian function can be proposed in order to fit experimental responses given in Figs. 1 and 3. Equation (3) is the proposed model for modeling the frequency of Current-Starved VCO as a function of both stage number and temperature. It is easy to demonstrate that substituting T=T_0=27°C the frequency-voltage characteristics is as Fig. 1a shows. Even more, if the control voltage is restrict to the range 2.2V≤V_{ctrl}≤4.2V the simplified model shown in (1) is reproduced. In a similar way, the whole model for the Schmitt Trigger VCO is given in (4), where applying identical conditions as before the response is as Fig. 1b shows and linearly limited by (2). Both mathematical models fit in high percentage experimental results into the range 1.0V ≤ V_{ctrl} ≤ 5.0V, however in order to estimate the relative error as function of the control voltage the result shown in Fig. 4 was obtained. From these graphs we can underline that the proposed fitting actually fit experimental data into the range 1.5V ≤ V_{ctrl} ≤ 5.0V. Furthermore, from data shown in Fig. 4 we can conclude that the major fitting error between Current-Starved VCOs (5.1%) is obtained

from the 9-stage oscillator at 35 °C. However, by including the fitting error of the another VCO circuit the higher error between both proposal is obtained from the Schmitt Trigger VCO and corresponds to 7.4% at T_0. In fact, such difference is due to the fitting approach because both architectures were fitted according to the same function. So, proposing a better fitting surely a lower error would be obtained. However, the purpose of the fitting models is to offer a design model that allow to the designer estimate the circuit performance under severe work conditions. For example, Fig. 5a shows the response given by (3) from **n**=3 to **n**=15 at T_0. On the other hand, Fig. 5b depicts the expected response to several oscillator circuits at T=100 °C, where the linear range is shifted to major control voltages as the number of stage decreases.

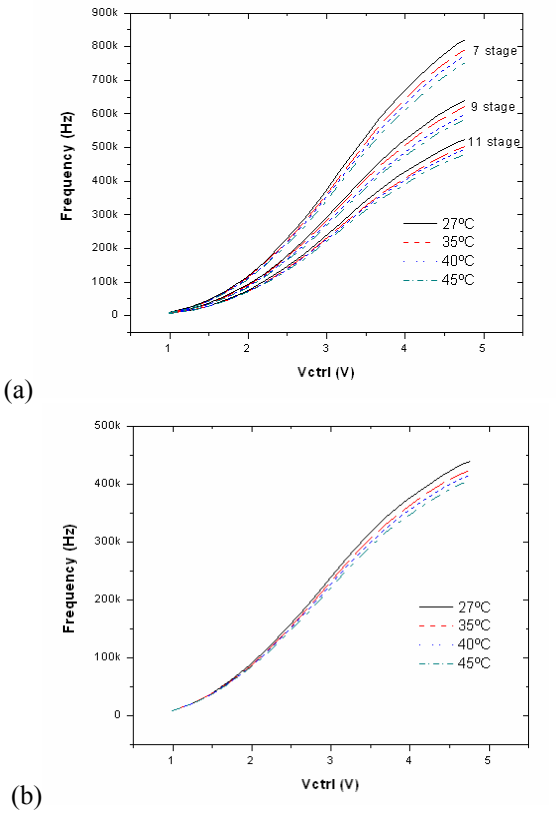


Fig. 3 Experimental response of VCOs for $T \geq T_0$. Current-Starved (a) and Schmitt Trigger (b).

4. ANALYSIS OF RESULTS

The test chip, shown in Fig. 6, includes not only VCOs but also MAGFETs, and poly-poly capacitors. The ATE's capabilities were evaluated by testing oscillator circuits. In order to measure the frequency f_{osc} several PSoC's modules were configured, i.e. with help of a timer and a 16-b PWM was possible count how many cycles of the measured signal ran during a 1sec window. That test process was done for each ΔV=244mV, where ΔV is the increment defined by the user in order to sweep the control voltage from V_{MIN} to V_{MAX}. Next, even when standard uncertainties decreased because of the high number of measurements, there are undesirable influences in experimental data because wide pulse signals not represent the dynamic characteristics of digital circuits; self-heating is presented in the frequency-voltage characteristics shown in both Fig. 1 and Fig. 3. The proposed fitting based on a gaussian approach, however, is a useful design model for both the IC designer and hand-work analysis. In order to evaluate the usefulness of the proposed ATE, we have looked at three basic issues: the test time, the error measurement, and the test methodology. We analyzed test time and error measurement in order to obtain circuits' performances under several work conditions in short test times. Test time is an important parameter mainly when the circuit's complexity increases. We also consider the scalability of this proposal to major architectures through the addition of lab equipment.

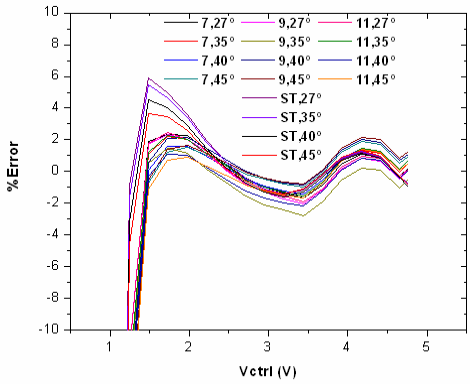


Fig. 4 Current-Starved and Schmitt Trigger relative error of the proposed fitting for $T \geq T_0$.

- ***Test time*** is limited by both the intermodules communications and external resources. However, the major test time is found once data is downloaded to the PC. The test time for obtaining the response shown in Fig. 1b, from the chip connection step to the graph visualization consumes of the order of 1min.

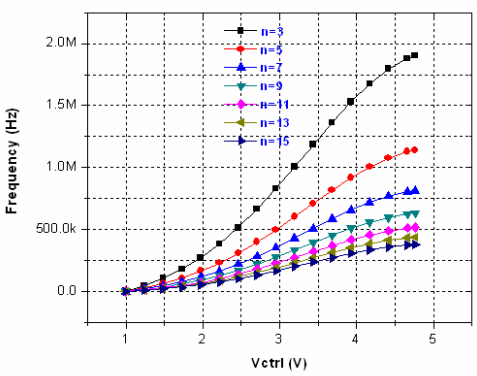
- ***Error measurement*** minimization must considere that various influences, acting together with measured value, result in difference between measured and true values of the measured quantity. In that sense the ATE corrects systematic influences by adding routines that define suitable test methodologies. The same is true when master-slave configurations are added. That sounds good but it is basic to estimate the uncertainty of the reading in order to avoid influencing q uantities surpass intervals defined by the manufacturer.

- ***Test methodology*** based on a network approach was defined in order to optimize resources [**6**] and also to reduce the error of method commonly found in trainees.

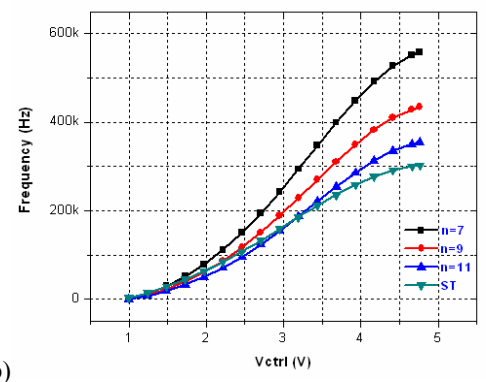
Currently a series interface is used to connect the ATE to a PC by using a RS-232 interface. However, it is well-known that a GPIB interface presents more advantages because more than 10 instruments can be connected.

$$f_{osc} = -\left(\frac{310.407x10^3}{N}\right)\cdot\left[-0.0038\cdot T + 1.1005 - \left(-0.084\cdot T + 21.874\right)\cdot Exp\left(-\left(0.426\cdot V_{ctrl} - 2.138\right)^2\right)\right] \quad (3)$$

$$f_{osc} = -49.712x10^3\cdot\left[-0.0042\cdot T + 1.1119 - \left(-0.0409\cdot T + 10.902\right)\cdot Exp\left(-\left(0.3755\cdot V_{ctrl} - 1.8556\right)^2\right)\right] \quad (4)$$



(a)



(b)

Fig. 5 Estimated VCOs' performance. Current-Starved at T_0 only (a); both VCOs at T=100°C (b).

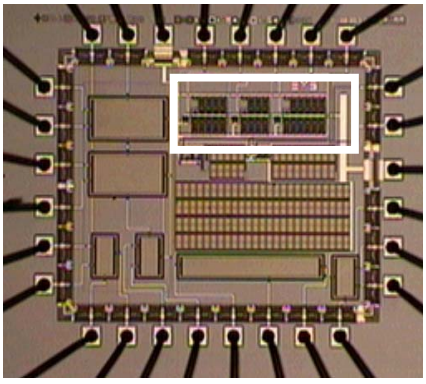


Fig. 6 Photograph of the test chip. Oscillator circuits are indicated at the top, right hand.

5. CONCLUSIONES

In this paper experimental data of Current-Starved and Schmitt Trigger VCOs were presented. These results for $T \geq T_0$ were obtained with help of a home-made automatic test environment (ATE). Since the ATE provides quality results by optimizing internal/external resources and communication protocols between them, an analytical model for reproducing the performance of VCOs as a function of temperature was proposed. The model, which follows a gaussian approach, reproduces in high percentage experimental data. The model was also used to estimate the VCOs' performance to higher temperatures. The proposed model is simple, non-complex and useful for the IC designer and also for hand-work analysis. Finally, from the experimental point-of-view, the higher relative error was obtained from the Schmitt Trigger VCO.

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