Soft-hardware Logic Circuit Design for a Four Bits Input Using MOS Floating-Gate Devices

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Abstract — **In this work, simulations using PSpice for a circuit with logical external configuration are presented used floating-Gate Transistor, where the design consists of a version needing no digital-to-analog converter at the input, as was reported in previous works. It is shown that this single circuit is able to process logic functions, configuring gates as: AND, OR, NAND, NOR, Exclusive-NOR, Exclusive-OR, with a properly calculated set of external voltages, connected to the corresponding programmable inverters. With this new circuit, the implementation of logic gates reduces considerably the number of transistors, as compared with conventional MOS logic gates.**

Keywords — **floating-gate transistor, logical external configuration circuit, CMOS, logical functions, neu-MOS, pre-input-gate inverter, FPD, programmable inverter.**

I. INTRODUCTION

First formally conceived in 1967, MOS floating gate transistor is formed by an electrically isolated gate and a control gate. Through the time, this first device has been well studied, such that new and optimum designs were reported in literature and implemented in practical systems. Such is the case of the so called neu-MOS (or νMOS) since it resembles the behavior of a biological neuron, as it has more than one control gate, then functionally representing a weighted sum of all the inputs signals connected to the control gates, at the floating gate. As a methodology, it presents a means for implementing a non-volatile memory element in silicon CMOS technology when the charge on the floating gate is to be modified. This is not the case in circuits as those presented in this work, since the condition needed for the operation of the gates, is to have no charge at all. Although floating gates are primarily used as storage in digital systems, there has been a trend of research and development over the last 15 years, for using them as an analog circuit element [1, 2, 3, 4, 5, 6, 7]. Such is the case reported in [8, 9], where Soft-hardware circuits based on neu-MOS transistor are presented. There, logic gates are implemented such that with only one circuit configuration, all of the Boolean functions can be handled, changing only external voltages depending on the desired logic gate.

The concept of theoretical FPD (Floating-gate Potential Diagram) of the logical functions is presented and simulated using PSpice, corresponding to the equivalent expected response of the logic function considered. A circuit that represents logic functions such as XOR, NAND, NOR, AND, OR and XNOR, etc., can be implemented by adjusting external control signals without any modifications in it, and is presented. The FPD is used for the gate performance prediction, applied to the floating gate of the νMOS inverter, shown in Fig. 1. Firstly we draw an FPD pattern to represent the desired logic function. Then the threshold of a pre-input-gate inverter (i.e., inverter A) and the values of coupling capacitances are determined from the abscissa and ordinate of the FPD, respectively. One main objective is to reduce the number of transistors through the elimination of the D/A converter shown in Fig. 1, using the FPD.

In this case, the design is done for a 4-b input function, establishing the magnitud of coupling capacitances and external voltages necessary for each of the studied gates.

In section 2 of this paper, the methodology of design for a circuit with a logical external configuration is presented, as well as the standards of design for the coupling capacitances used in the neuron circuit, programmable inverters and pre-input-gate inverter. Also, the FPD is described in detail. Section 3 will present the simulation for one of the gates considered, simulated both in DC and transient behaviors, together with the table of external voltages applied to the programmable inverters, in order to obtain the respective logic functions. Section 4 presents the conclusions of this work, and a suggested application for the designed circuit.

II. METHODOLOGY

The configuration of a neuMOS logic circuit is presented in Fig. 1. The circuit receives binary signals X_1, X_2, X_3 and X_4 as the input and gives a binary signal output, V_{OUT}. This particular circuit, given as an example, represents the XOR function of X_1, X_2, X_3 and X_4. The output stage of the circuit is a neuron circuit and is composed with a 6 input-gates complementary neuMOS inverter and a conventional inverter, whose function is to give logic 0´s and 1´s, as with a conventional digital circuit [10, 11]. The input stage of the circuit is a complementary νMOS source follower [11] which serves as a single-stage D/A converter. This circuit converts a 4-b binary input signal, X_1, X_2, X_3 and X_4, into a sixteen-level analog signal, V_p, which is named as a principal variable. This variable V_p, is also fed to inverters A, B, C, D, E and F (Fig. 1). The simulations of the circuit in Fig. 1, can be seen in [12, 13].

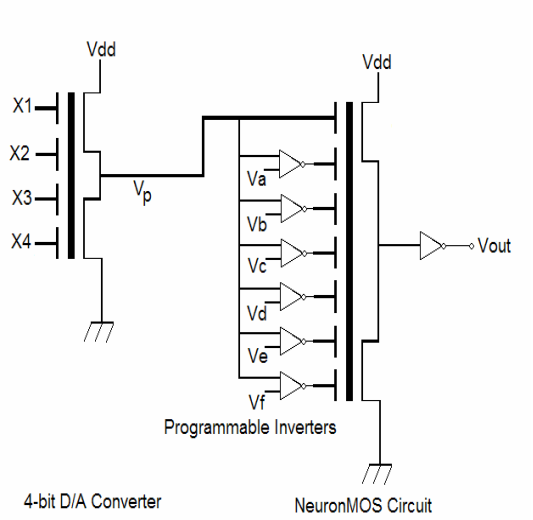

Fig. 1. Configuration of νMOS binary-logic, where the circuit is designed to implement logical functions.

The basic configuration of νMOS logic circuits presented in Fig. 1, employs a D/A converter circuit at the input stage which translates the combination of binary input signals into a single multivalued variable V_P. Then, the design of a νMOS binary-logic circuit reduces to the definition of a functional form of the so-called universal literal function in terms of multivalued logic. Such interpretation of νMOS logic circuits is quite straightforward and easy to understand, and in particular, is most suited for explaining the design principles. This is the reason why we have retained the D/A converter throughout the explanation in this paper. However, the D/A converter could be eliminated without any major disadvantages [8, 9]. The FPD for Fig. 1 is present in Fig. 2, where the *y-axis* is the floating-gate potential and the *x-axis* corresponds either to the analog value, Vp, from 0 Volts to V_{DD} (base line, Fig. 2), or to its digital equivalence for each of the sixteen possible combinations with 4-b.

It should be noticed in Fig. 2, that the *x-axis* is divided into 16 subdivisions. This is useful in terms of the determination of the threshold for the programmable inverters and this is derived from the number of input bits, as follows:

$$\#\,subdiv._{(x\text{ - axis})} = 2^N$$

Where *N* is the number of bits considered. Also, the number of subdivisions in the *y-axis*, should be:

$$\#\,subdiv._{(y\text{ - axis})} = 2 * 2^N$$

from where the magnitude of the coupling capacitances can be determined.

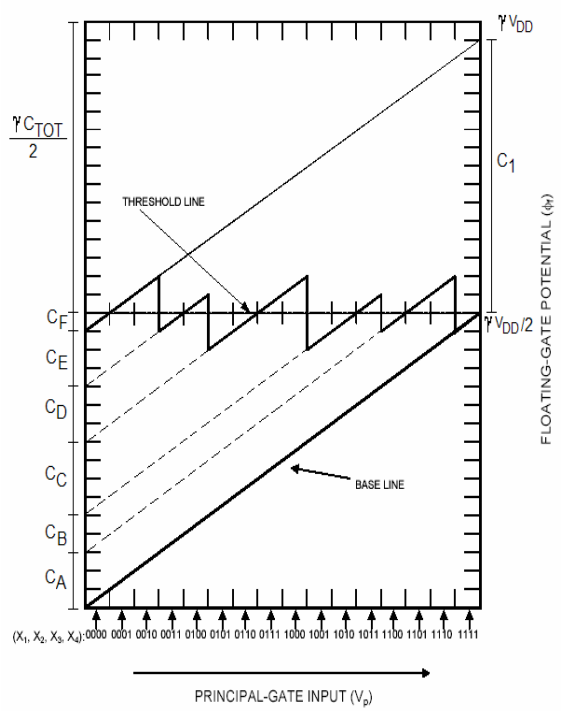

Fig. 2. Theoretical Floating-gate Potential Diagram (FPD) for the main νMOS inverter in Fig. 1. XOR logic function.

A. The Standard Design for the Coupling Capacitances of the neuron circuit.

With regard to the FPD of the previous figure, the coupling capacitances of the neuron are graphically determined as follows:

$$C_{X_1} = \frac{1}{32}\gamma C_{TOT} \qquad C_A = \frac{3}{32}\gamma C_{TOT}$$

$$C_{X_2} = \frac{2}{32}\gamma C_{TOT} \qquad C_B = \frac{2}{32}\gamma C_{TOT}$$

$$C_{X_3} = \frac{4}{32}\gamma C_{TOT} \qquad C_C = \frac{4}{32}\gamma C_{TOT}$$

$$C_{X_4} = \frac{8}{32}\gamma C_{TOT} \qquad C_D = \frac{3}{32}\gamma C_{TOT}$$

$$C_E = \frac{3}{32}\gamma C_{TOT}$$

$$C_F = \frac{1}{32}\gamma C_{TOT}$$

The D/A converter-less version of the exclusive OR (XOR) circuit is shown in Fig. 3, in which the configuration of the pre-input-gate inverter (with input signals Vp, Vc2 and Vf) is explicitly shown (to be compared with the circuit diagram in Fig. 1). The four input signals X_1, X_2, X_3 and X_4 are directly coupled via C_{X1}, C_{X2}, C_{X3} and C_{X4}, to the floating gates of the two νMOS inverters, having a weight ratio of 1:2:4:8, respectively.

Eliminating the D/A converter stage, simplifies the circuit configuration, thereby improving the integration density as well as the speed performance, while with a slight penalty of increased number of interconnects.

Fig. 3 shows that the configuration of the pre-input-gate inverter (input Vf, inverter F) is explicitly shown (to be compared with the circuit diagram in Fig. 1), where this circuit can readily operate without the D/A converter as the input stage, thus reducing the number of transistors needed and also eliminating a critical technological characteristic of the D/A converter transistors [8].

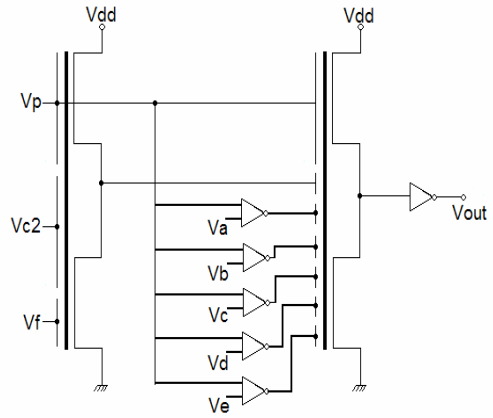

Fig. 3. Exclusive-OR circuit for four input variables X_1, X_2, X_3 and X_4: the D/A converter-less version of the circuit shown in Fig. 1.

B. The Standard Design for the Coupling Capacitances of programmable inverters and pre-input-gate inverter.

For the layout of programmable inverters, we should consider the possible minor technological dimension of capacitances, in order to avoid devices that could not be integrated in silicon foundries. Therefore, for the programmable inverters, it is convenient to consider C_O=C_{X1}, as the smallest capacitance, according to the following design approach:

$$C_{X_2} = 2C_{X_1}$$
$$C_{X_3} = 4C_{X_1}$$
$$C_{X_4} = 8C_{X_1}$$
$$C_{VC2} = C_{X_1} + C_{X_2} + C_{X_3} + C_{X_4}$$
$$C_{TOT} = C_0 + C_{X_{1..4}} + C_{VC2}$$

III. SIMULATIONS

The simulations were done using PSpice, with the level7 model for MOS transistors, using the technological parameters of the 1.2μm AMIS technology. Figs. 4a and 4b demonstrates the simulation results where the circuit's output (V_{OUT}) is shown as a function of the analog input signal, Vp [15, 16]. The first graph shows the DC simulation of the external configuration logic circuit and the second graph shows the transient simulation. The same was done for every function mentioned earlier, with satisfactory results also, with Vout as should be in each logic gate. Thus, the methodology outlined here, has been demonstrated to apply also to a converter-less version, and with a 4-b input. Besides, as mentioned in the first section, the number of transistors needed for implementing the logic function, is greatly reduced, improving hence, the integration area.

Example:XOR function. This Boolean function presents five inversion thresholds (Fig. 4a) but six coupling capacitances, where the inversion voltages of programmable inverters (V_A, V_B, V_C, V_D, V_E and V_F) are 3/16Vdd, 5/16Vdd, 9/16Vdd, 12/16Vdd and 15/16Vdd, 16/16Vdd respectively.

A circuit design hint derived from the Floating-gate Potential Diagram (FPD), is the number of programmable inverters, depending on the number of transitions present in the FPD, this is, how many times Φ_F crosses through $\gamma V_{DD}/2$, and the number of input coupling capacitances derived, out of those used for input signals. Here, the simulation of the FPD with PSpice is presented in Fig. 4a, where the correct behavior of the circuit is confirmed.

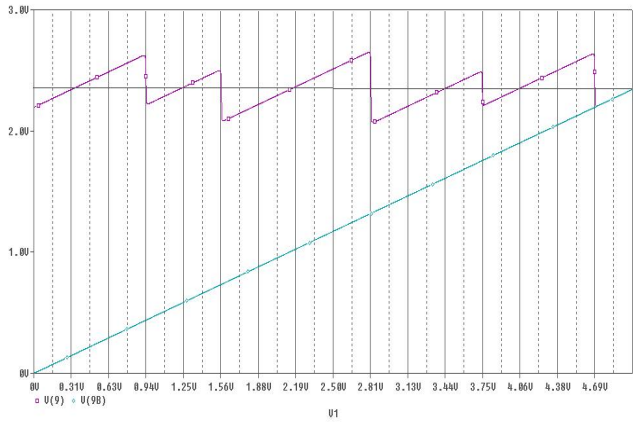

Fig. 4a. Simulated FPD for an Exclusive-OR circuit for four-input variables X_1, X_2, X_3 and X_4: the D/A converter-less version of the circuit shown in Fig. 3. DC Simulation.

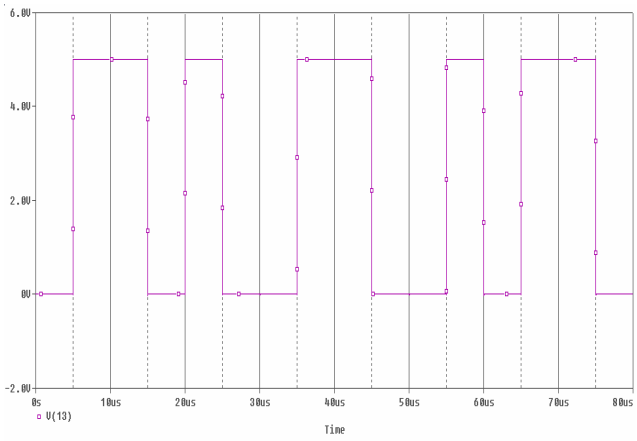

Fig. 4b. Simulated output response for an Exclusive-OR circuit with four input variables X_1, X_2, X_3 and X_4. Transient simulation.

Table I shows all the applied voltages to the programmable inverters, corresponding to the respective inversion thresholds of the programmable inverters for the six logic functions considered.

TABLE I. External voltages applied to the programmable inverters.

Function Logic	Corresponding external voltages of the programmable inverters						
	V_A	V_B	V_C	V_D	V_E	V_F	V_{C2}
XNOR	7.54V	6.6V	5.67V	4.42V	3.78V	5V	0V
NOR	7.54V	7.54V	7.54V	7.54V	7.54V	0V	5.26V
AND	7.9V	7.9V	7.9V	7.9V	7.9V	7.9V	0V
NAND	3.16V	3.16V	3.16V	3.16V	3.16V	0V	0.89V
OR	0V	0V	0V	0V	0V	0V	7.9V
XOR	3.17V	4.11V	5.04V	6.29V	6.92V	0V	8V

IV. CONCLUSION

The concept for logic external configuration circuits based upon a theoretical FPD for logical functions was presented. It is possible to simulate with PSpice, the behavior of a Soft-hardware logic gate, with design standards derived form the so called FPD graph. The results obtained, correspond to the expected response for the logic function considered, in this case, for a 4-b input signal. The same circuit can perform several logic functions such as XOR, NAND, NOR, AND, OR and XNOR, by just adjusting external control signals without any modifications to the circuit configuration, and good performance was obtained for all of them.

From a practical point of view, the original FPD representation, like the one shown in Fig. 2, is much easier to use in designing this kind of logic circuits. Therefore, the following procedure can be applied. First, draw an FPD pattern that matches the target function, then derive the coupling capacitances from the FPD graph axes; calculate the external voltages applied to the programmable inverters, depending on the logic function desired, and finally simulate the circuit, observing their behavior.

A future application of this circuit is the development of arithmetic circuits, i.e, adders and multipliers. This could lead to the design of an ALU with parallel processing, for instance.

REFERENCES

[1] Schwartz, D. B., Howard, R. E., and Hubbard, W. E., "A programmable analog neural network chip," *IEEE Journal of Solid-State Circuits*, Vol. 24, No. 2, pp. 313-319, 1989.

[2] Kub, F. J., Moon, K. K., Mack, I. A., and Long, F. M., "Programmable analog vector matrix multipliers," *IEEE Journal of Solid-State Circuits*, Vol. 25, No. 1, pp. 207-214, 1990.

[3] Shibata, T. and Ohmi, T., "A functional MOS-transistor featuring gate-level weighted sum and threshold operations," *IEEE Transactions on Electron Devices*, Vol. 39, No. 6, pp. 1444-1445, 1992.

[4] Ramirez Angulo, J., Choi, S. C., and Gonzalez Altamirano, G., "Low-voltage circuits building-blocks using multiple-input floating-gate transistor," Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on] Volume 42, Issue 11, Nov 1995 Page(s):971 – 974.

[5] Minch, B. A., Diorio, C., Hasler, P., and Mead, C. A., "Translinear circuits using sub-threshold floating-gate MOS transistors," *Analog Integrated Circuits and Signal Processing*, Vol. 9, No. 2, pp. 167-179, 1996.

[6] Hasler, P. and Lande, T. S., "Overview of floating-gate devices, circuits, and systems," IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing, Vol. 48, NO. 1, January 2001.

[7] Ramirez-Angulo, J. and Lopez, A. J., "Mite circuits: The continuous-time counterpart to switched-capacitor circuits," *IEEE Transactions on Circuits and Systems II-Analog and Signal Processing*, Vol. 48, No. 1, pp. 45-55, 2001.

[8] T. Shibata and T. Ohmi, "Neuron MOS Binary-Logic Integrated Circuits- Part I: Design Fundamentals and Soft-Hardware-Logic Circuit Implementation", *IEEE Trans. On Electron Devices*, Vol. 40, No. 3, pp.570-576, March 1993.

[9] T. Shibata and T. Ohmi, "Neuron MOS Binary-Logic Integrated Circuits- Part II: Simplifying Techniques of Circuit Configuration and Their Practical Applications", *IEEE Trans. on Electron Devices*, Vol. 40, No. 5, pp.974-979, May 1993.

[10] T. Shibata and T. Ohmi, "An Intelligent MOS transistor featuring gate level weight sum and threshold operations", *IEDM Tech. Dig.*, p. 919, 1991.

[11] T. Shibata and T. Ohmi, "A functional MOS transistor featuring gate level weight sum and threshold operations", *IEEE Trans. on Electron Devices*, Vol. 39, No. 6, pp.1444-1455, June 1992.

[12] A. Medina-Santiago and M. A. Reyes-Barranca, "Circuit for Logical-binary Functions using MOS Floating-gate Devices," 2do International Conference on Electrical and Electronics Engineering and XII Conference on Electrical Engineering, 2005.

[13] A. Medina-Santiago and M. A. Reyes-Barranca, "Convertidor D/A con Dispositivos de Compuerta Flotante," 9a. Conferencia de Ingeniería Eléctrica, Septiembre 3-5, 2003, pp. 127-130.

[14] J. Ramírez-Angulo, G. González-Altamirano, "A New Programmable Logic Family Using Multiple-input Floating-Gate Transistor", IEEE 1997.

[15] J. Ramírez-Angulo, G. González-Altamirano, "Modeling Multiple-input Floating-Gate Transistor for Analog Signal Processing", *IEEE International Symposium on Circuits and Systems*, June 9-12, 1997, Hong Kong.