# Implementation of an Adaptive Ultra-Low Power Time Delay Measurement ASIC

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***Abstract*—** Power dissipation from a low power integrated circuit is reported. The IC implements an adaptive version of the cross-correlation derivative algorithm for the estimation of inter-aural time difference. The architecture and logic structure as well as measured results reporting the performance of the IC -fabricated in a standard CMOS 0.5µm process- are shown.

## 1. INTRODUCTION

Several techniques such as Independent Component Analysis, Cross-correlation analysis [1],[10], Gradient Flow techniques [14], and the emulation of the human hearing cochlea [10], [4], [15], can be used for the localization of acoustic sources. Indeed, a number of analog and digital VLSI circuits have been successfully demonstrated in [10] [4][2][3][15], yet only a few of them have been designed to satisfy power consumption restrictions. Van Schaik and Shamma [15] report an integrated circuit (IC) based on the analog model of a human cochlea with a power dissipation that varies between 400 µW and 1.85 mW depending on the input signal. Stanacevic and Cauwenberghs [14] propose the analog processing of a signal at a sampling rate of 16 kHz, which can discriminate delay differences down to 2 µs, with a power consumption of 32 µW. Several realizations based on the cross-correlation derivative algorithm as proposed in [5] are reported in [6] and [8]. This method is a variation of the measurement of the inter-aural time difference (ITD) or time of flight between signals, which reduces the complexity of the calculations, and therefore is well suited for low power operation. The version presented in [8] is a 1.5mm × 3mm IC fabricated on a standard 0.5µm CMOS process that can discriminate delay differences down to 5µs with a power consumption of 12 µW at 2 V.

In this paper, we propose an alternative realization for the cross-correlation algorithm that reduces power consumption still further, while keeping calculation performance. The cross-correlation derivative (CCD) approach is a variation of the standard time-domain cross-correlation between two signals. The CCD algorithm works with a one bit discrete quantization of the input signals, and therefore, reduces drastically the complexity of the resulting digital circuitry. Another feature is that the spatial derivative of the cross-correlation is calculated instead of the cross-correlation itself. Calculation of the CCD results in an activity reduction of a thousand times in the digital circuitry. In the case of the standard cross-correlation approach, once the partial correlations are calculated, the maximum needs to be evaluated which requires a dedicated stage. In the CCD, it is only necessary to locate a change in the output value of the partial correlations (which are either 1 or 0), making this task trivial: one only needs to detect transitions of the input signals. The strategy proposed in this paper uses a single counter for delay measurement together with an adaptive closed loop system. The closed loop guarantees stability, and also a convergence of the count to the delay under measurement. The reduction of power consumption is a consequence of the reduction in size of the circuitry. In fact, just one counter for the whole ASIC is needed as opposed to the previous versions [6] and [8] where one counter per delay tab was needed. Section II depicts the system's basic digital architecture. Section III shows the final results of the ASIC functional verification and offers a comparison of its's power dissipation against several of the alternative implementations discussed earlier.

## 2. STRUCTURAL DESIGN (FRONT-END)

### 2.1. Basic Structure

Figure 2 depicts the basic structure of the architecture: a block that captures the signals being measured, and another block which calculates the delay. Delay is given by a two's complement index, with two extra signals that provide information about the state of the unit: *out_range* and *data_rdy*.

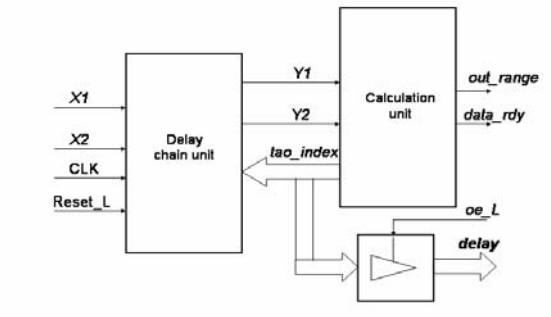


Figure 1. Block diagram of front-end design

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### 2.2. Delay Chains

The first block, shown in Figure 2, captures the signals at a 200 kHz rate. This rate was fixed due to previous design constraints [5]. Data is stored in two Serial In-Parallel Out (SIPO) registers that serve as delay chains. Considering such speeds, the circuit proposed would allow for the measurements of delays up to ±640 μs.

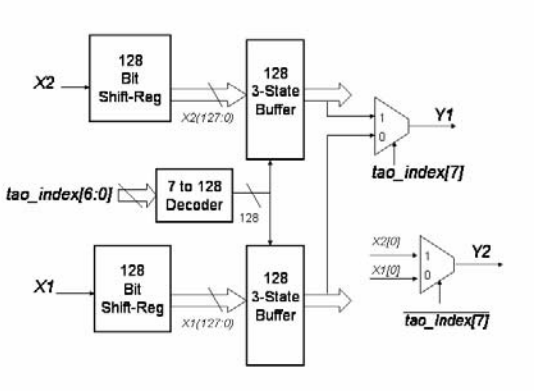


Figure 2. Block diagram of the delay chain

For reference's sake, it is always assumed that signal X1 leads X2. The first bit of one of the chains (by convention X2) is used as base pointer, while the other chain is swept in search of transitions by the signal *tao_index*. This index is an 8-bit signed integer in two's complement. The sign bit switches the multiplexers in the case where X1 is actually lagging X2, instead of leading it. Thus, the base pointer is switched to X1[0] and the index's magnitude is used to sweep X2.

### 2.3. Calculation Unit

The calculation unit in Figure 3 must discover valid transitions in the input signal to account for an increase or decrease of the index counter, depending on the index sign bit. Repeated application of the calculation will produce a monotonic estimation of the target delay. Since the circuit is designed to increase or decrease its count by one on each valid transition, the convergence time is determined by:

$$T_{convergence} = \frac{1}{2} * \frac{f_{CLK}}{f_{signal}} * \left| Delay_{current} - Delay_{new} \right| \quad (1)$$

where $\left| Delay_{current} - Delay_{new} \right|$ is the absolute signal delay change from a steady state measurement to the new value of delay to be measured, that is, the difference between the current delay and the delay value that the system has to reach. An *out_range* signal is provided to indicate the saturation of the index counter. This serves as an auxiliary signal to allow for the adaptive measurement of faster or slower signals via the modification of the clock's speed.

For the validation of the transitions, the signals pass through two registers (Figure 2. ). The decision logic determines whether to increase, decrease or leave the counter unchanged depending on the arrival order of the transitions and variable *tao_index* current state. Transitions are checked on the rising and falling edges of the input signals. Evaluation thus occurs at a speed twice as fast as the signal's frequency (on a noise-free signal). The decision logic is registered in order to eliminate the chance of falsely locking the circuit to the same transition. This avoids a run-up in the counter.

## 3. Functional Verification and Implementation

### 3.1. Functional Simulation and FPGA Testing

Simulations were run at the RTL level and the gate level (with back annotation from the post placement and routing models generated by ISE®). Results from the ModelSim® simulator were fed into Matlab® for a preliminary check of the accuracy of the method. A set of files with test signals was created in Matlab® to serve as stimulus signals to the simulator. The system was prototyped on a FPGA for preliminary verification, as stated in [16].

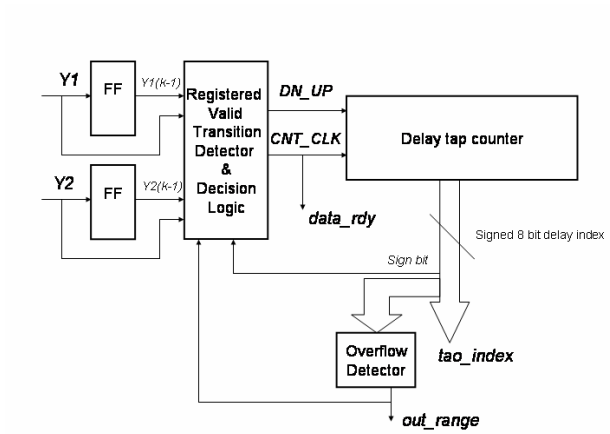


Figure 3. Computing of the index for the delay chains (delay between X1 and X2)

### 3.2. VLSI Realization

A VLSI implementation was done using Tanner® CAD tools. A SPICE model was extracted for its simulation on Mentor Graphics® Eldo and Mach-TA for analog timing checking, power estimations and digital verification. Considering its size and operational speed, the Delay Chain unit is the responsible for the maximum power dissipation. In order to minimize power consumption, the SIPO delay chains were built using $C^2$MOS registers. This master-slave edged triggered register does not need feedback, because the data is stored in the internal node capacitances, and features a lower clock fan-in and a smaller area of only eight transistors versus the eighteen transistors required for a typical static register [11].

Figure 4. shows the complete layout of the chip with a photographic detail of a $C^2$MOS register. The ratio between PMOS and NMOS transistor was set to 1.9 to reduce the delay chain's size. From the viewpoint of power consumption, the calculation unit is not as critical as the delay chains because in the worst-case condition (maximum delay between X1 and X2), the counter operates at a maximum speed equal to twice the input signal frequency, which is supposed to be a low frequency signal. However, efforts were made to keep logic and registers at a minimum; whenever possible, all transistors were set to minimum size (being the PMOS 3 μm by 0.6 μm and the NMOS 1.8 μm by 0.6 μm). Eldo Spice simulations of the circuit without pads at 2.7 V gave as result a total power consumption of 11 μW.

The IC was fabricated in a standard 0.5µm CMOS technology with 3 metal layers and 2 poly layers.

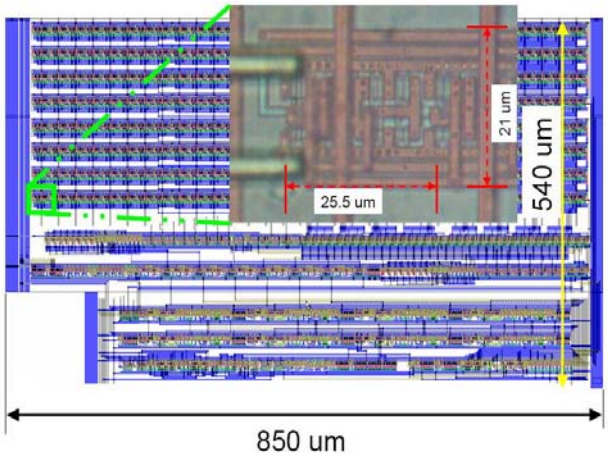


Figure 4. IC layout

## 4. Digital Functional Verification and Measurement

A testbench for the functional verification of the IC was written in Verilog HDL and implemented on a Digilent Inc. Spartan 3 Board. The system is centered on a Xilinx® PicoBlaze® embedded microcontroller that interfaces the unit with the user and it is able to generate different delays between two 200 Hz reference signals. Both delayed signals are supplied by a programmable delay generator with a step size of 2.5µs. The delays are either pre-programmed using a look-up table or taken from the pseudo-random sequential vectors provided by a LFSR register. A software routine checks that the delays are within the IC measurement range. The different delays are sequentially and asynchronously fed to the IC at a time rate of 1 second per vector. This allows for full convergence of the IC to a steady state. The IC output bus is read at a 1.25ms sampling rate, which provides a long enough interval for the measurement of at least 200 samples of the target delay estimation in steady state. Data is taken from the testing board and fed to a PC with Matlab via RS-232. Figure 5. shows the convergence time for a reference delay change among 480 µs, -635 µs and 67.5 µs. The IC output converges according to time prediction (1) in both cases. When the reference is not an integer of the base time (5µs) the output will oscillate between the two closest values. This can be seen in Figure 5. in the case where the reference delay is 67.5 µs: the output changes between 65 µs and 70 µs indicating a precision of ± ½ bit.

Figure 6. shows 100 time series of measured delay at the IC output data bus. The delay of each signal pair was chosen from a range between -700 µs and +700 µs. As can be observed, the IC always reaches steady state with a convergence speed of one sample /5µs. Some out of range signals were fed to the system, to test for its recovery out of the saturation stage, which was satisfactory in all cases.

An HP-34401A voltmeter was used to measure power consumption data from each power pin. Table 2 compares data with reports from other implementations: a significant improvement is observed in all cases.

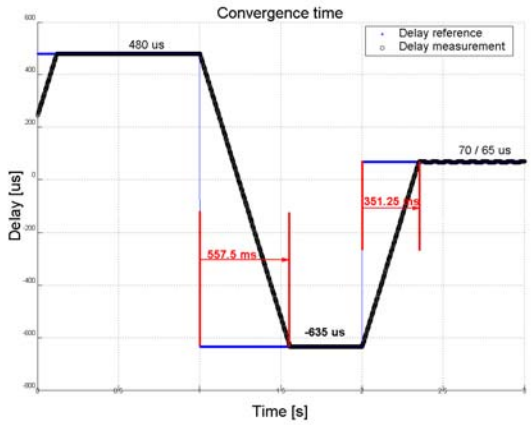


Figure 5. Convergence time

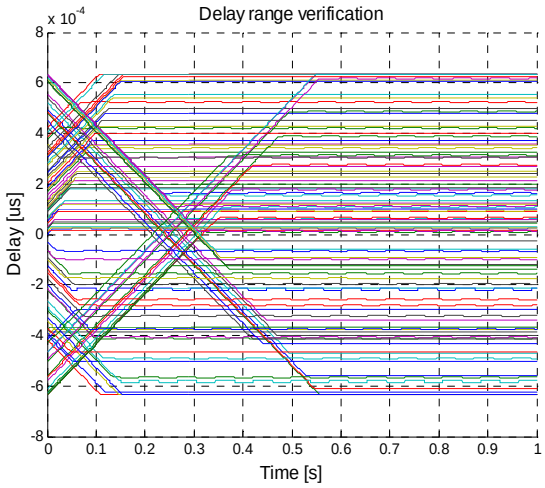


Figure 6. Delay input range verfication

Table 2. Comparison of total power consumption between systems

| Unit | Area | Tech. (µm) | VDD (V) | Total Unit Power (uW) | Power saving factor |
|---|---|---|---|---|---|
| Neuromorphic sound localizer (Schaik, 2004). | 5mm x 5mm | 0.50 | 3.3 | 1850 | 150.4 |
| Micropower gradient flow (Stanacevic, 2005 ) | 3mm x 3mm | 0.50µm | 3 | 54 | 4.4 |
| Cross-correlator (Julián, 2006). | 2mm x 2.4mm | 0.35µm | 3.3 | 300 | 24.4 |
| Adaptive ASIC | 1.5mm x1.5mm | 0.50µm | 2.7 | 12.3 | 1 |

## 5. CONCLUSIONS

A realization of an ASIC for the calculation of the delay between two digital signals has been presented.

Verification tests showed that the ASIC is functional and exhibits an extended range that allows for measurement of delays up to ±640 μs with a sampling speed of 200 kHz. The circuit was implemented in an IC fabricated using a standard CMOS 0.5 μm technology. Electrical measurement results showed a significant improvement in total power dissipation over other implementations, reaching 12.3 μW. The efficiency of $C^2$MOS dynamic techniques was thus corroborated, with new improvements being still possible by reducing supply voltage in the critical stages.

## 6. ACKNOWLEDGEMENTS

This work is partially funded by "Desarrollo de tecnología de redes de sensores para aplicaciones en el medio social y productivo", PICT 2003 No. 14628, Agencia Nacional de Promoción Científica y Técnica; "Redes de Sensores" PGI 24/ZK12, Universidad Nacional del Sur; "Desarrollo de Microdispositivos para Redes de Sensores Acústicos", # 5048, PIP 2005-2006, CONICET. A. Chacón-Rodriguez is on a scholarship funded by the Organization of American States, and the Instituto Tecnológico de Costa Rica. The authors also want to thank The MOSIS Service for chip fabrication.

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