MODELING AND ESTIMATING LEAKAGE CURRENT IN PASS TRANSISTOR LOGIC NETWORKS

Paulo F. Butzen[1], André I. Reis[2], Renato P. Ribas[1]

[1]Instituto de Informática – UFRGS, Porto Alegre, Brazil
[2] Nangate Inc. – Menlo Park, CA, USA

{pbutzen, rpribas}@inf.ufrgs.br, are@nangate.com

ABSTRACT

This paper reviews the modeling of subthreshold leakage current and proposes an estimation method for pass-transistor logic circuit. The estimation method takes into account the subthreshold current at the output buffer as well as in the logic network, where only single off-transistors are responsible for the standby current during the steady state analysis. The proposed leakage model has been validated through spice simulation, considering an 130nm CMOS technology, with good correlation of the results.

1. INTRODUCTION

The desire to achieve high integration density has resulted in aggressive transistor scaling. In the same way, the supply voltage is scaled to reduce the power. However, the performance is proportional to the ratio V_{dd}/V_{th}. In order to maintain the circuit performance, the threshold voltage is scaled down. The transistor threshold voltage is associated with an exponential increase in subthreshold leakage current. As a result, the subthreshold current is one of the main responsible for power dissipation in advanced CMOS technologies. Consequently, the identification and estimation of leakage current is very important in designing low power circuits.

In this sense, pass-transistor logic – PTL represents an interesting alternative in the design of digital VLSI circuits, especially when high performance and low power applications are targeted. A number of different PTL styles have been proposed in the literature, for instance CPL [1], EEPL [2], SRPL [3], although the most efficient solution seems to be the combined CMOS/PTL approach [4] to explore the best features of each one in the final circuit – the current-drive capability and noise margin of CMOS, and the speed and low power consumption of PTL.

On the other hand, several subthreshold leakage models to purely series and parallel off-transistors arrangements are known [5]-[7]. However, no one has evaluated the leakage current in PTL style.

This paper evaluates the static consumption in PTL networks and the restoration circuits (output buffers). The subthreshold leakage model is presented in Section 2. Section 3 discusses the leakage estimation for different PTL approaches, while the standby current estimation at the output circuit is analyzed in Section 4. Section 5 gives some experimental results proving the validation of the proposed model. Finally, the conclusions are presented in Section 6.

2. LEAKAGE MODEL

The total leakage dissipation results from the sum of the current in each branch of off-transistors between the supply voltage and ground. To present the proposed method the off-network illustrated in Fig. 1 can be considered as the entire NMOS pull-down arrangement. The same analysis is applicable to a PMOS pull-up tree.

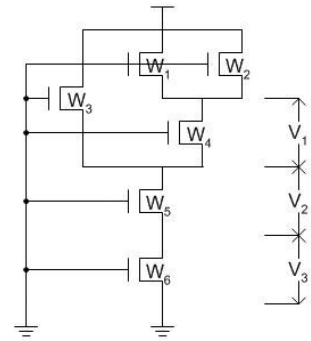

Figure 1 - NMOS series-parallel network.

From the BSIM MOS transistor model [8], the subthreshold current for a MOSFET device can be modeled as

$$I_S = I_0 W e^{\frac{V_{gs}-(V_{t0}-\eta V_{ds}-\gamma V_{bs})}{nV_T}}\left[1-e^{-\frac{V_{ds}}{V_T}}\right] \quad (1)$$

where $I_0 = \frac{\mu_0 C_{ox} V_T^2 e^{1.8}}{L}$ and $V_T = \frac{kT}{q}$. V_{gs}, V_{ds} and V_{bs} are the gate, drain and bulk voltage of the transistor respectively. V_{t0} is the zero bias threshold voltage. W and L are the effective transistor width and length, respectively. γ is the body effect coefficient and η is the

DIBL coefficient. C_{ox} is the gate oxide capacitance, μ_0 is the mobility and n is the subthreshold swing coefficient.

The subthreshold current through the top devices, i.e. transistors connected to V_{dd}, can be expressed by equation (2). This equation considers the variable V_j as the voltage across every transistor placed below the top transistor in the stack.

$$I_{Si} = I_0 W_i e^{\frac{-\sum V_j - [V_{t0} - \eta(V_{dd} - \sum V_j) + \gamma \sum V_j]}{nV_T}} \quad (2)$$

The subthreshold current through the other transistors in the network is expressed by equation (3). The differences between both equations are observed in the η expression (DIBL effect) and in the last term, which can be eliminated when $V_i >> V_T$. Again, V_j represents the voltage across every transistor below the node in the stack.

$$I_{Si} = I_0 W_i e^{\frac{-\sum V_j - [V_{t0} - \eta V_i + \gamma \sum V_j]}{nV_T}} \left[1 - e^{-\frac{V_i}{V_T}} \right] \quad (3)$$

The voltage across the transistors can be evaluated in three different situations. The subsequent analysis assumes that $V_{dd} >> V_i$, which drop out all the V_i terms. It also considers the fact that $V_i >> V_T$, so that the (V_i/V_T) term can be ignored.

The first situation is represented by the voltage V_1 in Fig. 1. In this case, it is possible to associate every transistor connected in that node by series-parallel association. The terms W_{above} and W_{below}, in the equation (4), represent the width of the transistor above and below the node V_i, respectively. For this condition, V_i is given by

$$V_i = \frac{\eta V_{dd} + nV_T \ln\left(\frac{W_{above}}{W_{below}}\right)}{1 + 2\eta + \gamma} \quad (4)$$

The second situation, in turn, is presented by the voltage V_2 in Fig. 1. In this condition, it is not possible to make series-parallel associations between the transistors connected at *i*-index node. The term V_{above} in the following equation represents the voltage of the transistors above the node V_i. For this state, the voltage V_i is given by

$$V_i = \frac{nV_T \ln\left(\frac{\sum W_{above} e^{\frac{\eta V_{above}}{nV_T}}}{W_{below}}\right)}{1 + \eta + \gamma} \quad (5)$$

Finally, the third situation is represented by the voltage V_3 in previous example. This case only happens at the bottom transistors and the analysis cannot assume $V_i >> V_T$, so that the term exp(-V_i/V_T) should not be ignored. To simplify the mathematic calculation, the term $e(-V_i / V_T)$ in (3) can be expressed by $(1 - V_i / V_T)$. Then, V_i is obtained by equation (6), where $C = 1 + \eta + \gamma$.

$$\frac{C}{n}\left(\frac{V_i}{V_T}\right) + \ln\left(\frac{V_i}{V_T}\right) = \frac{\eta V_{above}}{nV_T} + \ln\left(\frac{W_{above}}{W_i}\right) + \ln\left(\frac{V_{above}}{V_T}\right) \quad (6)$$

3. PASS TRANSISTOR LOGIC STYLE

In pass-transistor logic style, usually some input signals are connected to the source/drain node of a MOS transistor (logic switch), instead of in the transistor gate as occur in standard CMOS cells. The advantages are the smaller number of transistors and the smaller input loads [9]. Considering these two characteristics, PTL circuits should be faster and dissipate less power than traditional CMOS logic style. However, since the output level is lowered by threshold voltage in case of 'high' state through NMOS device, it is necessary to restore the level up to V_{dd}. Similar behavior occurs when low logic level in transmitted through a PMOS switch. To restore the voltage levels, an output buffer is added at the end of the PTL network. This restoration block also provides a better output driving capabilities, increasing in penalty the circuit area and power dissipation.

It is possible classify the PTL networks in two subgroups: single-rail structures and dual-rail ones, also known as differential pass-transistor logic - DPTL. Differently from single-rail networks, where is necessary to add inverters for generating the complemented signals, dual-rail approaches present all signals duplicated in the circuit connections. Logic and routing area overhead is the main cost attached to such feature. Several DPTL propositions are motivated to simplify the restoration block, as illustrated in the next section.

The first PTL approaches were composed only by NMOS switches. As previously discussed, the NMOS transistor generates a voltage drop in the case of high logic level. To mitigate this effect it is possible to alternate NMOS and PMOS transistors to find a better solution, as proposed in [10]. Another solution to avoid the voltage drop is to use transmission gates.

In order to evaluate the subthreshold leakage current in PTL networks, it is important to remember that such logic style is building using the concept of multiplexers, which present a unique behavior related to leakage current. For all possible input combination, the leakage transistors can be isolated and treated as single off-transistors. Off-transistor stacks, strongly desired in standard CMOS gates in terms of static consumption, are not observed in PTL networks. Fig. 3 illustrates a PTL 4-input multiplexer – MUX_4x1, and the leakage currents for one input combination.

Fig. 4 presents all NMOS transistor behavior in a PTL network. Fig. 4a represents the on-transistor states. When power supply (V_{dd}) is applied in one side, the other terminal is lowered by threshold voltage (V_{th}). In the case that the voltage applied in the source terminal is already dropped by V_{th}, the drain terminal keeps the same

condition. Fig. 4b, in turn, presents the off-transistor behavior. As previously presented in equation (1), the subthreshold leakage current depends exponentially on the transistor source-drain voltage (V_{ds}). Based on this statement, the subthreshold leakage for the first, second, and third cases can be ignored because it is orders of magnitude smaller than the leakage current in the last two cases. The same analysis is suitable to PMOS transistor networks.

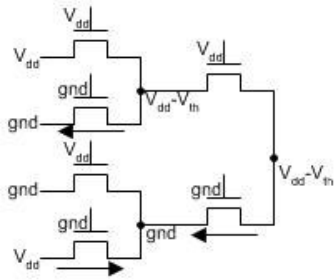

Figure 3 – PTL 4-input multiplexer.

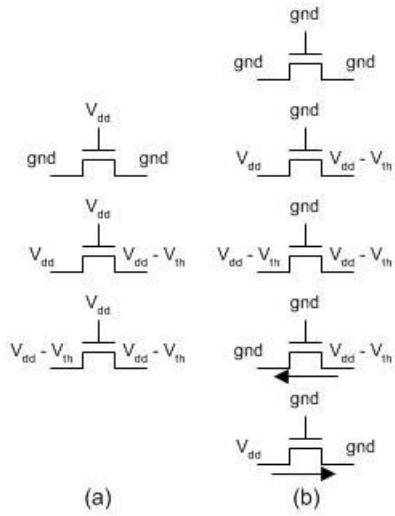

Figure 4 – NMOS switch electrical behavior.

4. RESTORATION CIRCUITS

The main goal of the output buffer is to restore the voltage drop from the logic network. This circuit provides also acceptable driving capability to the next logic block. The simplest circuit that attends these characteristics is the inverter. However, as the NMOS pass-transistor network drops the voltage when it is in high state, the output inverter for such high input (V_{dd} - V_{th}) presents a short circuit current, since the PMOS transistor is in linear region and the NMOS transistor in saturated region. To solve this undesired behavior, the directly solution is add a keeper to restore the inverter input voltage. Most of the circuits reported in the literature use the output inverter and the keeper device in different arrangements. Some works present variations in order to speed-up the circuit, where the keeper is composed by a stack of transistors, at the expense of power dissipation [11]. Other approaches try to reduce the consumption by using just the keeper without the output inverter [10]. This configuration avoids the leakage at the output circuit but does not provide the driving capability to the next stage. The restoration circuit proposed in [3] reduces the leakage current by eliminating the keepers and taking advantage of the dual-rail style to restore the signal.

Fig. 5 presents several PTL 2-input multiplexer, with different restoration circuits reported in the literature.

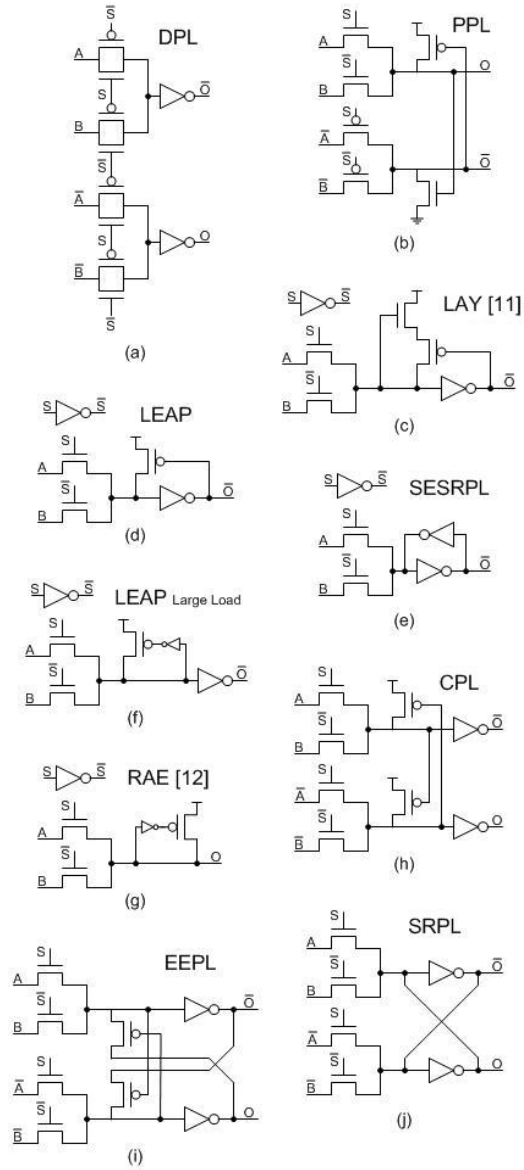

Figure 5 –Different PTL approaches: 2-input multiplexer.

5. SIMULATION RESULTS

In order to validate this work, the results obtained from the proposed model were compared to Hspice simulation, considering commercial 130nm CMOS

process parameters and operating temperature at 100°C. To simplify the analysis transistors with equal sizing were applied, although the device size is a parameter in the model. The leakage current was calculated and correlated with Hspice results for several 2-input multiplexer logic styles, depicted in Fig 5. The results presented in Table 1 and Table 2 show a good agreement between the analytical model and the simulation data, showing an absolute average error less than 2%.

6. CONCLUSIONS

A subthreshold leakage current model has been presented to be applied in Pass Transistor Logic circuits. The PTL networks and the restoration circuits have been evaluated independently. The proposed model has been validated considering a 130nm CMOS technology, in which the subthreshold current is the most relevant leakage mechanism and the results present a good accuracy.

7. REFERENCES

[1] K. Yano, "A 3.9ns CMOS 16x16-b Multiplier using Complementary Pass-Transistor Ligic", IEEE J. Solid-State Circuits, vol. 25, no. 2, pp. 1145-1151, Apr. 1996.

[2] M Song, "Design of a Low Power 54x54-bit Multiplier Based on a Pass-transistor Logic", Proc. Int. Electronics, Circuits and Systems Conference, 1998, pp. 51-56.

[3] A. Parameswar, H. Hara, T. Sakurai, "A High Speed, Low Power, Swing Restored Pass-Transistor Logic Based Multiply and Accumulate Circuit for Multimedia Applications", Proc. IEEE Custom Integrated Circuits Conference, 1994, pp. 278-281.

[4] Y. Wan, M. Shams, "Optimization of Mixed Logic Circuits with Application to a 64-bit Static Adder", Proc. Int. VLSI Design Conference, 2005, pp. 261-166

[5] R. X. Gu and M. I. Elmasry, "Power Distribution Analysis and Optimization of Deep Submicron CMOS Digital Circuit", IEEE JSCC, vol.31, no.5, pp.707-713, May 1996.

[6] Z. Cheng, M. Johnson, L. Wei and K. Roy, "Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling of Transistor Stacks", Proc. Int. Symp. Low Power Electronics and Design, 1998, pp. 239-244.

[7] S. G. Narendra and A. Chandrakasan, "Leakage in Nanometer CMOS Technologies", Springer, 2006.

[8] B. J. Sheu, D. L. Scharfetter, P. K. Ko, M. C. Jeng, "BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors", IEEE J. Solid-State Circuits, vol. SC-22, no. 4, Aug. 1987.

[9] R. Zimmermann, W. Fichtner, "Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic", IEEE J. Solid-State Circuits, vol. 32, no. 7, pp. 1079-1090, Jul. 1997.

[10] W. H. Paik, H. J. Ki, S. W. Kim, "Push-Pull Pass-Transistor Logic Family for Low-Voltage and Low-Power", Proc. Europ. Solid-State Circuits Conf. , 1996, pp. 116-119.

[11] Y. Lai, Y. Jiang, H. Chu, "BDD Decomposition for Mixed CMOS/PTL Logic Circuit Synthesis", Proc Int. Symposium on Circuits and Systems, 2005, pp. 5649-5652.

[12] G. Rae, R. Chen, "Synthesis of Single/Dual-Rail Mixed PTL/Static Logic for Low-Power Application", IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, vol. 23, n. 2, pp. 229-242, 2004.

[13] J. Pihl, "Single Ended Swing Restoring Pass Transistor Cells for Logic Synthesis and Optimization", Proc Int. Symposium on Circuits and Systems, 1998, pp. 1141-1144.

Table 1. Input dependence leakage estimation (nA) in PTL logic circuits from Fig. 5.

Input	CPL[9]		EEPL[9]/SRPL[3]		DPL[9]		PPL[10]		LEAP[9]/RAE [12]		LEAP L. L.[9]		LAI [11]		SESRPL[13]	
(SAB)	Hspice	Prop.	Hspice	Prop.	Hspice	Prop.	Hspice	Prop.	Hspice	Prop.	Hspice	Prop.	Hspice	Prop.	Hspice	Porp.
000	17.9	17.7	13.1	13.1	13.1	13.1	21.5	21.5	21.5	21.3	29.8	29.6	16.7	16.8	21.5	21.3
001	34.5	34.3	29.8	29.6	39.3	39.0	29.8	29.8	21.5	21.3	26.2	26.0	165.0	166.8	29.8	29.6
010	34.5	34.3	29.8	29.6	39.3	39.0	29.8	29.8	29.8	29.6	38.3	38.3	25.0	25.2	29.8	29.6
011	17.9	17.7	13.1	13.1	13.1	13.1	21.5	21.5	13.1	13.1	17.8	17.3	13.1	13.1	21.5	21.3
100	17.9	17.7	13.1	13.1	13.1	13.1	21.5	21.5	17.8	17.3	26.2	26.0	13.1	13.1	21.5	21.3
101	34.5	34.3	29.8	29.6	39.3	39.0	29.8	29.8	26.2	26.0	34.5	34.3	21.5	21.5	29.8	29.6
110	34.5	34.3	29.8	29.6	39.3	39.0	29.8	29.8	17.8	17.3	22.6	22.5	161.2	163.1	29.8	29.6
111	17.9	17.7	13.1	13.1	13.1	13.1	21.5	21.5	9.5	9.4	13.1	13.1	9.6	9.4	21.5	21.3

Table 2. Maximum, minimum and average leakage for 2-input MUX implemented in different PTL approaches.

PTL Logic Style	Maximum Leakage			Minimum Leakage			Average Leakage		
	Hspice	Proposed	Error (%)	Hspice	Proposed	Error (%)	Hspice	Proposed	Error (%)
CPL [9]	34.5	34.3	0.6	17.9	17.7	1.1	26.2	26.0	0.8
EEPL [9] / SRPL [3]	29.8	29.6	0.7	13.1	13.1	0	21.5	21.4	0.5
DPL [9]	39.3	39.0	0.8	13.1	13.1	0	26.2	26.1	0.4
PPL [10]	26.2	26.0	0.8	0	0	0	13.1	13.1	0
LEAP [9] / RAE [12]	21.5	21.3	0.9	9.5	9.4	1.1	19.7	19.4	1.5
LEAP L. L. [9]	38.3	38.3	0	13.1	13.1	0	26.0	25.9	0.4
LAI [11]	165.0	166.8	1.1	9.6	9.4	2.1	53.2	53.6	0.9
SESRPL [13]	29.8	29.6	0.7	21.5	21.3	0.9	25.6	25.5	0.4