

DESIGN STRATEGY OF CURRENT SOURCE IN CURRENT-STEERING CMOS DAC

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ABSTRACT

A new design strategy of current sources in CMOS current-steering segmented digital-to-analog converter (DAC) used into a RF transmitter stage for 2.45GHz Bluetooth applications, is presented. The design strategy is based on an iterative scheme which variables are adjusted by a simple way, satisfying the requirements and reaching the design specifications. A theoretical analysis of static and dynamic requirements for the current-steering DAC design is included. Some performance results obtained through simulations are: INL=0.25LSB, DNL=0.04LSB and SFDR=60dB ($F_{out}=1\text{MHz}$, $F_s=50\text{MHz}$). The DAC is designed and simulated in $0.35\mu\text{m}$ 4M2P CMOS technology.

1. INTRODUCTION

A DAC is used into a RF transmitter because digitally processed signals must be transmitted as an analog wave to other stations. The DAC design must fulfill specifications of: bandwidth, resolution, Spurious-Free Dynamic Range (SFDR), Signal-to-Noise Ratio (SNR) and Differential and Integral Nonlinearities (INL, DNL). These specifications are determined by the modulation standard of the RF transmission stage. Also, low power and reduced area are required conditions to implement portable systems. Good dynamic performance, high speed and moderate resolution digital-to-analog converters are used in RF transmitters to generate the modulation signals. Current-steering segmented architecture is suitable for this application [1]. It is based on an array of matched current sources that are switched to the output. In a

current-steering segmented DAC the digital word (N-bits) is divided in N_{bin} least significant bits (LSBs) which control the binary weighted current sources, and N_{seg} most significant bits (MSBs) to control $2^{N_{seg}} - 1$ unary weighted current sources using a binary-to-thermometer decoder. As a result, on the output node the current sum generates a voltage according to the digital word. NMOS transistors were selected for the cascode current sources design and PMOS transistors (M_{SW}) for the differential switch pair (Fig. 1).

Current sources design in a CMOS current steering segmented DAC determines the static and dynamic behavior. However, in the literature a lot of works do not pay attention to a good selection of current source structures and design style, neither; thence, final INL and DNL values are adjusted iteratively without take them into consideration previously. Consequently, a good current sources design must consider the finite output resistance of the DAC, which degrades INL, DNL and SFDR specifications. Also, thermal noise and quantization noise relation must be determined to obtain the required resolution, and the transistor sizes must be minimized to reach the speed specification without neglecting the dynamic behavior. Additionally, the geometric characteristics of the current sources must be selected to anticipate the mismatch effect on the transistor's V_t and β parameters, which may degrade the INL, DNL and SFDR specifications. As a solution, this work presents a design variables tradeoffs study to establish a simple strategy for current sources design in CMOS current-steering segmented DACs.

Design variables tradeoffs of the static and dynamic behavior and the specifications which must fulfill a DAC into Bluetooth standard are studied in Section 2. Section 3 presents the design strategy and it is applied to design a DAC which results are summarized in the Section 4 to draft some final conclusions.

2. DESIGN REQUIREMENTS

Design requirements in a given architecture are imposed by the specifications. This work traces a current-steering segmented DAC current sources design step by step supplying Bluetooth standard specifications. Therefore, it is important to present briefly the specifications.

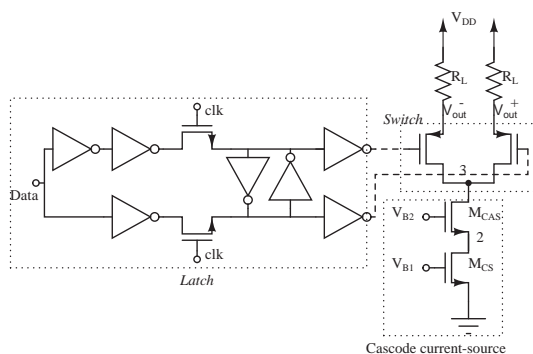


Fig. 1. Current cell circuit diagram

An RF transmission stage introduces spurious frequencies to the transmitted signal, then the DAC design must obtain a SFDR that overcomes the minimum allowed value (50dB). Conversion bandwidth must be equal or larger than the channel bandwidth (1MHz), because a minimum sampling frequency of $F_s = 2MHz$ is demanded. Due to the output signal characteristics of the converter, it is necessary a high analog filter in order to recover the desired signal. In order to reduce the filter order, it is required to make F_s larger than channel bandwidth [2]. In addition, monotonic behavior is guaranteed if the non-linearity specifications are: $INL < 0.5LSB$ and $DNL < 1LSB$ [1]. To know in detail the design variables we need to analyze the design requirements in advance to fulfill the Bluetooth specifications mentioned previously.

A. Finite output resistance

Within the current-steering architecture each current source has a finite output resistance associated with the output current value. The LSB current source will have the maximum output resistance and the MSB current source will have the minimum output resistance. Therefore, total output conductance depends on active sources number, and this characteristic change the waited output current according to the digital word ($X = b_0 + 2b_1 + 4b_2 + \dots + (2^N - 1) \cdot b_{N-1}$). The output current behavior due to this effect, is given by [1]:

$$I_{out} = \frac{I_{LSB} \cdot X + V_{DD} \cdot G_{LSB} \cdot X}{1 + G_{LSB} \cdot R_L \cdot X} \quad (1)$$

where I_{LSB} is the current LSB, G_{LSB} is the output LSB conductance and V_{DD} is the supply voltage. The difference between the actual current and the ideal current increases as X increases and the non-linearity specification (INL, DNL) will be larger. Consequently, it is necessary to obtain a G_{LSB} value that allows to fulfill the INL, DNL and SFDR requirements.

B. Mismatch error requirements

The mismatch errors generate variations statistically independent in V_t (threshold voltage) and in β (current factor) of the MOS transistors according to area, direction and distance of the transistors into the silicon wafer. The standard deviation of the drain-to-source current of a MOS transistor in saturation mode (of sizes $W \times L$) is given by [3]:

$$\sigma_{I_D}^2 = \frac{A_\beta^2}{\beta^2 W L} + \frac{4A_{V_t}^2}{(V_{B1} - |V_t|)^2 W L} \quad (2)$$

where A_{V_t} and A_β are constants that describe the variations of V_t and β respectively, they are provided by integrated circuit manufacturer. Drain-to-source current variations in the current sources generate INL and DNL components additional to the INL and DNL components due to finite output resistance mentioned before. In order to fulfill the INL and DNL specification, it is required to select an adequate value for N_{seg} using the equation [4]:

$$N'_{seg} = N + 1 - \log_2 \left[\left(\frac{\sigma_{DNL}}{2\sigma_{INL}} \right)^2 \cdot (2^N - 1) + 1 \right] \quad (3)$$

If the number of segmented bits is larger than N'_{seg} then $\sigma_{INL} > \sigma_{DNL}$, and if N_{seg} is less than N'_{seg} then $\sigma_{INL} < \sigma_{DNL}$. Additionally, the M_{CAS} and M_{CS} transistors (Figure 1) may operate in the triode region or cut-off region instead of the saturation region due to V_t and β variations in the MOS transistors. The design must foresee this situation through an adequate margin between the bias point and the maximum and minimum voltage which the M_{CAS} and M_{CS} transistors will operate in the saturation region and the differential switch pair operating in the triode region [3].

C. Quantization noise

The quantization noise in a current-steering differential DAC is uniformly distributed in the conversion bandwidth $0 < F < F_s/2$ with a Power Spectral Density $S_q(f)$. Also, a DAC is affected by the thermal noise, it is associated with the transistors and resistances that conform a current-steering DAC. When the quantization noise is less than the thermal noise the converter resolution is not equal to the bits number because the thermal noise magnitude exceeds the lower conversion levels. Therefore, it is not possible to include these levels into DAC resolution. During DAC design a value of I_{LSB} , V_{ov} and R_L is selected taken into account that the quantization noise exceed the thermal noise with a safety margin. A margin recommended in literature is $S_q(f) > 10 \cdot S_t(f)$, this value corresponds to a resolution loss of approximately 0.069 bits [4].

D. Settling time

Changes in the DAC output signal produced by variations in the digital word do not happen instantaneously due to parasitic capacitances. Therefore, it is necessary to define a settling time. If DAC sample time is larger than settling time then there will be conversion errors, because the output signal does not settle correctly. This effect limits the maximum sampling frequency. γ_2 is the ratio between the small-signal charge at the internal node 2 (Fig. 1) and at the output node $\gamma_2 = \frac{V_2(0)C_2}{V_{out}(0)C_{out}}$. Because the sizes of M_{CS} transistor are larger than the sizes of M_{CAS} transistor due to mismatch errors, then the small signal charge at the node 3 may be neglected. If the γ_2 value increases then the settling time diminishes, but the voltage peak during the current source switching transient increases. The contrary case happens when the γ_2 value is reduced. If the voltage peak has high power, spurious appears in the DAC's frequency response and the SFDR specification is degraded. Consequently, it will be necessary to find out the sizes of M_{CAS} and M_{SW} transistors (the size of M_{CS} transistor is established by mismatch requirement) in order to fulfill the settling time requirement without degrading the SFDR specification. The settling time becomes smaller if the channel width of the M_{CAS} and M_{SW} transistors will be smaller and the voltage peak will be larger [3].

3. DESIGN STRATEGY

In this section the DAC current sources design strategy to fulfill the design requirements, is explained. Additionally, a way to adjust variables to reach the Bluetooth specifications is presented. Fig. 2b shows the design strategy steps for current sources design which is described in this section.

A. N_{seg} Selection

The mismatch error requirements for DNL and INL specifications are used to select the number of unary weighted current sources N_{seg} . Equation 3 is used for this selection. The DNL and INL specifications have two static components: due to mismatch error and due to finite output resistance. In order to consider both components on INL specification suppose that the first half of the INL specification is product of finite output resistance and the other half is due to mismatch error. This supposition allows defining approximately the value of each component within the DNL and INL specification which was obtained through previous simulations. To know optimal proportion between INL component due to finite output resistance and INL component due to mismatch error imply to know before the transistor sizes. However, to know the transistor sizes, it is necessary to know the INL value. Nevertheless, the designer may to change this proportion in order to improve the design. Finally, the σ_{INL} value assumed into equation 3 will be equal to 0.25. The DNL component is smaller than INL component, considering the finite output resistance [1]. Thus, it is possible to neglect this component into DNL specification [1]. The σ_{DNL} value must be smaller than accumulated maximum value $\sum_{i=0}^{2^N-1} DNL_i = INL_i - INL_0 = 0.25$. If $N = 12bits$ and $\sigma_{INL} = 0.25$ is selected then $\sigma_{DNL} = 0.125$ obtains $N'_{seg} = 4.9$, if $\sigma_{DNL} = 0.0625$ then $N'_{seg} = 6.9$. In the state of art, the number of unary weighted current sources are between 4 and 7 bits [1].

B. Minimum area selection

Due to the mismatch error it is necessary to use a minimum area for the M_{CS} transistor into LSB current source that allows to fulfill the DNL and INL specifications [4]:

$$(WL)_{LSB} \geq \left(\frac{S}{2\sigma_{INL}} \right)^2 \cdot \left\{ \frac{A_\beta^2}{\beta^2} + \frac{4A_{V_t}^2}{(V_{B1} - V_t)^2} \right\} \cdot (2^N - 1) \quad (4)$$

Using this equation the minimum area for the M_{CS} transistor may be found depending on the voltage V_{B1} (Fig. 1). When V_{B1} is increased, the area is reduced of exponential way. However, If V_{B1} is high, it must use larger width so that M_{CAS} operates in the saturation region. The area reduction for $(V_{B1} - V_t) > \frac{2A_{V_t}\beta}{A_\beta}$ are not significant. Consequently, the designer may choose V_{B1} close to $\frac{2A_{V_t}\beta}{A_\beta} + V_t$ to obtain a design of low area, using a moderate value of V_{B1} . The V_{B1} voltage selection establishes the minimum area of the M_{CS} transistor to fulfill the nonlinearity specification due to mismatch error requirement (for a given value of A_β and A_{V_t}). If

the manufacture process has a high A_β and A_{V_t} values, it is necessary to use a high voltage V_{B1} or to use larger area for the current sources design, overcomes, the capacitances will be larger limiting the DAC's speed.

C. Load resistance selection

The load resistance selection must consider: if R_L is very large the DAC's bandwidth will be smaller because the pole in the output nodes is reduced, also the output resistance of the current sources must be elevated to fulfill the output resistance requirements of the INL, DNL and SFDR specifications. Therefore, the designer may to choose a small R_L value (around of 15Ω to 100Ω), in agreement with full-scale output voltage specification of the DAC design. That is to say, the designer may select a small value of R_L , but this value will be adjusted to reach the full-scale output voltage specification after of the I_{LSB} selection.

D. I_{LSB} current selection

A minimum current value for LSB current source exists due to quantization noise requirement. Using the values V_{B1} and R_L selected previously is calculated the minimum I_{LSB} . However, this current value may not be sufficient so that the design does not reach the bandwidth specification. Then it will be necessary to verify the specification fulfillment at the final design and to return to this point (to choose a larger current) if the bandwidth specification is not fulfilled (Fig. 2).

E. LSB output resistance selection

The equation 1 is used to calculate the LSB current source output resistance that allows to reach the INL and DNL specification. This calculation is made for the worst case INL ($X = 2^N - 1$) [1]. Therefore, using the INL definition $INL = (I_{out}(X = 2^N - 1) - I_{LSB} \cdot (2^N - 1))/2 \cdot I_{LSB}$, it is possible to find the G_{LSB} minimum for the INL specification by effect of finite output resistance. In this same way, it is selected the minimum G_{LSB} for the Nonlinearities specifications by effect of finite output resistance. On the other hand, it is necessary to verify that the selected output resistance for the LSB current source allows to obtain the SFDR specification. Fourier series coefficients of the output signal (equation 1 where $X = (2^N - 1)\sin(w_{out})$) to verify the SFDR specification is used [1].

F. M_{CS} design

In this step, it is due to select the M_{CS} transistor sizes for the LSB current source (according to the values obtained from I_{LSB} and $(WL)_{LSB}$) approximating these values through the first-order dc model of an NMOS transistor operating in the saturation region.

G. V_{B2} Selection

The bias voltage V_{B2} will have one minimum value in which M_{CS} does not operate in the saturation region (V_{B2}^{min}) and one maximum value in which M_{CAS} does not operate in the saturation region (V_{B2}^{max}). A good selection

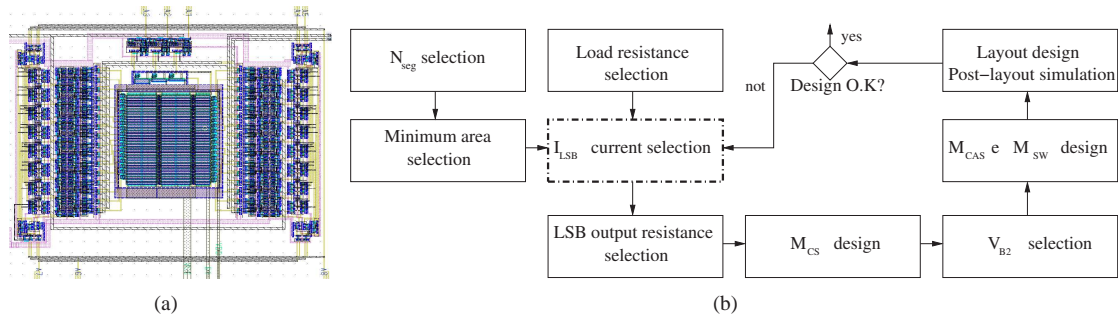


Fig. 2. (a) Layout (b) Design Strategy of the current sources

is the bias voltage in which the LSB current source output resistance is maximum. It is the midpoint between V_{B2}^{max} and V_{B2}^{min} , denominated V_{B2}^{opt} [3]. If V_{B2} is smaller than V_{B2}^{opt} , then the channel width of M_{CAS} transistor must be larger to operate in saturation mode reducing the DAC's bandwidth. The contrary case happens if V_{B2} is larger than V_{B2}^{opt} . Additionally, the designer must prevent that V_{B2} exceed the range $V_{B2}^{max} - V_{B2}^{min}$ due to mismatch error. Therefore, it is recommended to select V_{B2}^{opt} .

H. M_{CAS} and M_{SW} Design

In order to choose the sizes of these transistors, it is necessary to consider the following aspects: To guarantee that M_{CAS} and M_{SW} operate in the saturation region and in the triode region respectively, LSB current source output resistance must be $\approx 1/G_{LSB}$, the safety margin is $V_{B2}^{min} < V_{B2} < V_{B2}^{max}$, due to the mismatch error effect on the bias point of MOS transistors. Then, different values of the channel width for the M_{CAS} and M_{SW} transistors are tested using minimum channel length. In this way, it is possible to find the smallest channel whereas M_{CAS} and M_{SW} operate correctly. Next, a *Monte Carlo* simulation to verify the safety margin is made. Additionally, it is must verify that the LSB current source output resistance fulfills the required value (this test is only for the LSB current source). If it is not reached, the channel length of the M_{CAS} transistor may be increased. For the design of each current source the channel width of the M_{CS} transistor is increased in agreement with the current value, repeating the previous step for all the current cells.

Until this design stage only the static behavior was considered, trying to reduce the transistors sizes obtaining minimum channel width and minimum channel length. However, it is not the best choice to reduce the voltage peak of the transient behavior. The designer may adjust the sizes of M_{CAS} and M_{SW} transistors for trading-off between settling time and voltage peak. This will not be necessary if DAC's load capacitance is sufficient great so that the γ_2 value fulfills the settling time requirement. The load capacitance is constituted by the interconnection parasitic capacitances of $2^{N_{seg}} - 1 + N_{bin}$ current sources, the pad capacitance and the junction capacitance of the M_{SW} transistors. Therefore only after the layout implementation the load capacitance will be known. If the load capacitance value is supposed known, an I_{LSB} current that allows to reach the required bandwidth may

TABLE I
Summary of DAC post-layout simulation results.

Specification	Value
Resolution	8-Bit
Full-Scale Output Current	2mA
Output Resistance	50Ω
INL	0.25LSB
DNL	0.04LSB
Maximum Update Rate	50MS/s
SFDR* ($F_{out} = 1MHz$)	60dBc
SFDR* ($F_{out} = 5MHz$)	50dBc
* $F_s = 50MS/s$	

be determined in an iterative way by adjusting the voltage peak (Fig. 2). In this way, it is possible to minimize the DAC's power consumption.

4. POST-LAYOUT SIMULATION RESULT

The post-layout simulation results of designed DAC is shown in the table I. Since in the INL and DNL post-layout simulation the mismatch error was not considered, the INL and DNL component due to the mismatch error must be added. The Layout has been designed in $0.35\mu m$ 4M2P CMOS technology (Fig. 2a) accomplish through IC Station of Mentor Graphics. The final active area was $0.3mm^2$.

5. CONCLUSIONS

In this paper, the design strategy presented allows to design the current sources of a CMOS current-steering segmented DAC that fulfills the minimum specifications for the 2.45GHz Bluetooth applications. In order to fulfill the INL, DNL, SFDR, SNR and bandwidth specifications in the current steering segmented architecture, the proposed strategy lets quickly to adjust the design variables in a simple and iterative way.

6. REFERENCES

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