OPTIMAL DESIGN OF A CLASSICAL CMOS OTA-MILLER USING NUMERICAL METHODS AND SPICE SIMULATIONS

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ABSTRACT

We propose in this work an optimization procedure for the design of a classical OTA-Miller CMOS integrated circuit. Our approach is based on a multi-objective minimax formulation to achieve the desired design specifications by numerical optimization. A brief description of the OTA-Miller is realized, showing its simulated responses at the starting point. The optimization procedure is described, including the definition of the error functions in terms of the design specifications, as well as the formulation of the corresponding minimax multi-objective function. Finally, the simulated optimized responses are reported. Our procedure is general enough to be applicable for the optimal design of other basic analog CMOS circuits, and it makes use of readily available software tools.

1. INTRODUCTION

Analog circuit design usually starts from some well known topology that must satisfy a set of some given specifications under certain constraints. The problem of designing the circuit essentially consists of finding the best component parameter values that satisfy, ideally in an optimal way, the design specifications without violating any of the design constraints.

Typically, any change in the component values of the circuit directly affects one or more performance parameters, such that the complete circuit has to be analyzed after any change in order to validate that the circuit still satisfies all the required specifications. A practical solution to quickly predict the responses when changes are frequently applied consists of using CAD tools, such as SPICE.

The optimal design of CMOS integrated circuits usually requires the knowledge and skills of a specialist, who can roughly predict the circuit performance for each change applied to the circuit based on his experience and knowledge. However, when many conflicting design specifications are demanded from the circuit, even expert designers can benefit from the usage of numerical optimization procedures, especially those based on high-precision models for the circuit components, which are difficult to manipulate analytically during the design process.

We propose in this paper an optimization procedure for the design of a textbook CMOS OTA-Miller integrated circuit. Our approach is based on a multi-objective minimax formulation to achieve several conflicting desired specifications by using numerical optimization. A brief description of the classical OTA-Miller is first realized, showing its SPICE-simulated responses at the starting point. The optimization procedure is described, including the definition of the error functions in terms of the design specifications, as well as the formulation of the corresponding minimax multi-objective function. Finally, the SPICE-simulated optimized responses are reported, using high-level models for the CMOS transistors. Our procedure is general enough to be applicable for the optimal design of other fundamental analog integrated circuits, and it makes use of readily available software tools, such as Matlab[1] and WinSpice[2].

2. BRIEF DESCRIPTION OF THE OTA-MILLER

The schematic of a classical OTA-Miller integrated circuit implemented with CMOS transistors [1] is illustrated in Fig. 1. It consists of two amplification stages. The first stage is a basic differential pair implemented with PMOS transistors (M1 and M2), which has a single-ended current source as active load implemented with NMOS transistors (M3 and M4). This

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[1] MATLAB, Ver. 7.0.1 (R14), The MathWorks, Inc.
[2] WinSpice, Ver. 1.04.05, Dep. Elec. & Comp. Sci., U. of California, Berkeley.

stage is biased with the current mirror formed with PMOS transistors M5 and M6, whose reference current source is I_{REF}.

The second stage is a basic common source amplifier with an NMOS transistor (M7) acting as amplifier and a PMOS transistor (M8) acting as a current source load. This OTA-Miller is designed to drive a load capacitor, C_L, of 10pF. The second stage has a feedback compensation capacitor, C_c. This OTA-Miller is biased with voltage sources $V_{DD} = -V_{SS} = 2.5$V.

The process parameters for the transistors used in this work correspond to the AMI Semiconductor Technology Process SCN15 1.6µm. We use level 49 for the SPICE models of all the CMOS transistors during simulation [3].

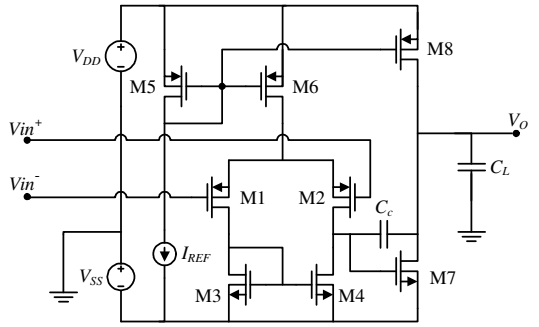

Fig. 1 Schematic of a classical CMOS OTA-Miller.

3. DESIGN SPECIFICATIONS AND STARTING POINT

Having selected the technology process, the design of our classical CMOS OTA-Miller integrated circuit starts by defining the design specifications in terms of the performance parameters of interest, such that the open loop voltage gain, *Av*, the phase margin, *PM*, the common-mode rejection ratio, *CMRR*, the slew rate, *SR*, the input common voltage range, *ICMR*, the power dissipation, *PD*, and the output voltage swing, O_{SW}. The design specifications required for our circuit are shown in Table I.

We assign the initial values indicated in Table II to the design variables. The corresponding SPICE responses of the magnitude and phase of *Av* are in Fig. 3.

We can see from Fig. 3 an initial |*Av*| at low frequencies of approximately 49dB, and the unitary gain frequency, f_T, of approximately 600KHz. On the other hand, the phase margin, *PM*, defined as the difference between the phase of *Av* read at f_T (−105° in this case) and −180°[1] is approximately $PM = 75°$.

The simulated common-mode rejection ratio, *CMRR*, is approximately 96.5dB (see Fig. 4).

The simulated positive slew rate, SR^+, is 2.14V/µs, while the SR^- is −2.21V/µs (see Fig. 5).

The simulated $ICMR^-$ is −2.44V, while the $ICMR^+$ is 1.85V (see Fig. 6).

[3] http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-abn/t22x-params.txt

TABLE I
DESIGN SPECIFICATIONS OF THE OTA-MILLER

Specification	Required	Initial	Optimized
|*Av*| (dB)	> 60	49	83.1
PM (°)	55 < *PM* < 70	75	58
CMRR (dB)	> 95	96.5	96
SR^+ (V/µs)	> 4	2.14	4.1
SR^- (V/µs)	> −4	−2.21	−4.1
ICMR (V)	> 3	1.8/−2.4	1.8/−2.4
O_{SW} (V)	> 4	2.2/−2.4	2.3/−2.4
PD (µW)	< 450	181.1	440.8

TABLE II
COMPONENTS VALUES FOR THE OTA-MILLER

Component	Initial	Optimized
$(W/L)_{1,2}$ (µm)	(26/16)	(21.6/16.2)
$(W/L)_{3,4}$ (µm)	(10/10)	(11.9/10.8)
$(W/L)_{5,6}$ (µm)	(13/10)	(12.3/14)
$(W/L)_7$ (µm)	(115/5)	(122.1/4)
$(W/L)_8$ (µm)	(55/5)	(62.9/4.5)
C_c (pF)	1	0.8183
I_{REF} (µA)	2.5	3.9

The output voltage swing (O_{SW}^+ and O_{SW}^-) are 2.13V and −2.46V, respectively (see Fig. 7).

Finally, the total power dissipation, *PD*, at the starting point is 181.8µW.

The initial responses of the OTA-Miller are summarized in the third column of Table I. It is seen that the initial design violates some of the specifications.

4. OPTIMIZATION PROCEDURE

4.1. General Description

The problem consists of finding the optimal values of the design variables to achieve the desired performance of the circuit. The optimization variables are: the transistor lengths and the widths, L_k and W_k respectively, for $k = 1$ to 8, the compensation capacitor, C_c, and the reference current, I_{REF}. This optimization variables are assembled in vector $\boldsymbol{x} \in \Re^{18}$, where $\boldsymbol{x} = [L_1 \ldots L_8, W_1 \ldots W_8, C_c, I_{REF}]$. The flow diagram illustrated in Fig. 2 summarizes the optimization procedure and is next described.

We start by defining the initial values of the optimization variables, as well as the specifications (this part is described in the previous section).

The second block generates a SPICE netlist of the classical OTA-Miller from the numerical software tool (e.g. Matlab). In the third block, the SPICE simulation is done and results are saved in a readable output file (e.g. results.csv) for the numerical software tool.

The fourth block reads the output file. In the fifth block, the simulated results and the specifications generate an error whose maximum value is sent to the next block.

The sixth block decides if criteria of termination are satisfied and stops if necessary, otherwise, continues.

Finally, the seventh block predicts the new iterate based on the optimization method used, that is, it calculates the next value of vector $\boldsymbol{x}$ that will be simulated.

4.2. Error Function Definition

The error function formulation used in the fifth block of the flow diagram in Fig. 2 (objective function calculation) consists of comparing the simulated responses with the specifications, making a positive error when the specification is violated, and a negative error if the specification is satisfied. The error function for each specification is next described and is also summarized in Table III.

The first error, e_1, ensures a minimal $|Av|$ of 60dB at low frequencies. If $|Av|$ is smaller than $|Av|_{\min}$ = 60dB, it means that the specification has been violated, and then the value of e_1 will be positive.

The second error, e_2, is for the upper limit of the phase margin, while e_3 is used for the lower limit of *PM*. Errors e_2 and e_3 are intended for keeping the *PM* between 55° and 70°. φ_{un} is the voltage phase read at the unitary gain frequency, f_T.

The corresponding error for the *CMRR* is e_4, to ensure a $CMRR_{\min}$ = 95dB.

Errors e_5 and e_6 are used to ensure a minimal *SR* of 4V/µs, that is, $SR^+_{\min}$ = 4V/µs and $SR^-_{\min}$= −4V/µs.

Errors e_7 and e_8 are used to guaranty an *ICMR* of 3V, that is, $ICMR^+_{\min}$ = 1.5V and $ICMR^-_{\min}$ = −1.5V.

The O_{SW} specification is assigned to errors e_9 and e_{10} to ensure at least 4V of output voltage swing, that is, $O_{SW}{}^+_{\min}$ = 2V and $O_{SW}{}^-_{\min}$ = −2V.

Error e_{11} keeps *PD* lower than 450µW, that is, $PD_{\max}$ = 450µW.

Error e_{12} avoids I_{REF} to be lower than 1µA, that is, $I_{REF\_\min}$ =1µA.

In the optimization procedure, the compensation capacitor, C_c, can take a positive or negative value. Thus, to ensure a positive value we set the restriction for C_c to be at least 0.01pF, that is, $C_{c\_\min}$ = 0.01pF. Its assigned error is e_{13}.

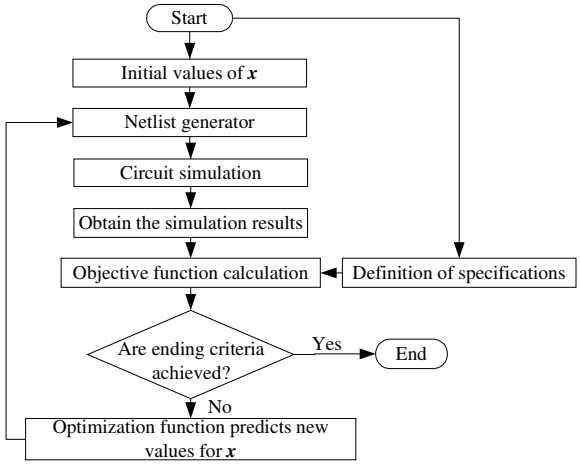

Fig. 2 Flow diagram for the optimization procedure.

TABLE III
ERROR FUNCTIONS FOR THE OTA-MILLER

i	e_i	Limits
1	$1 - \lvert Av\rvert/\lvert Av\rvert_{\min}$	$\lvert Av\rvert_{\min}$ = 60dB
2	$\varphi_{un}/\varphi_{un\_\max} - 1$	$\varphi_{un\_\max} = -125°$
3	$1 - \varphi_{un}/\varphi_{un\_\min}$	$\varphi_{un\_\min} = -110°$
4	$1 - CMRR/CMRR_{\min}$	$CMRR_{\min}$ = 95dB
5	$1 - SR/SR^+_{\min}$	$SR^+_{\min}$ = 4V/µs
6	$1 - SR/SR^-_{\min}$	$SR^-_{\min}$ = −4V/µs
7	$1 - ICMR/ICMR^+_{\min}$	$ICMR^+_{\min}$ = 1.5V
8	$1 - ICMR/ICMR^-_{\min}$	$ICMR^-_{\min}$ = −1.5V
9	$1 - O_{SW}/O_{SW}{}^+_{\min}$	$O_{SW}{}^+_{\min}$ = 2V
10	$1 - O_{SW}/O_{SW}{}^-_{\min}$	$O_{SW}{}^-_{\min}$ = −2V
11	$PD/PD_{\max} - 1$	$PD_{\max}$ = 450µW
12	$1 - I_{REF}/I_{REF\_\min}$	$I_{REF\_\min}$ = 1µA
13	$1 - C_c/C_{c\_\min}$	$C_{c\_\min}$ = 0.01pF
14	$1 - W_{1\text{-}2}/W_{1\text{-}8\_\min}$	$W_{1\text{-}8\_\min}$ = 4µm
15	$1 - L_{1\text{-}2}/L_{1\text{-}8\_\min}$	$L_{1\text{-}8\_\min}$ = 1.6µm
16	$1 - W_{3\text{-}4}/W_{1\text{-}8\_\min}$	$W_{1\text{-}8\_\min}$ = 4µm
17	$1 - L_{3\text{-}4}/L_{1\text{-}8\_\min}$	$L_{1\text{-}8\_\min}$ = 1.6µm
18	$1 - W_{5\text{-}6}/W_{1\text{-}8\_\min}$	$W_{1\text{-}8\_\min}$ = 4µm
19	$1 - L_{5\text{-}6}/L_{1\text{-}8\_\min}$	$L_{1\text{-}8\_\min}$ = 1.6µm
20	$1 - W_7/W_{1\text{-}8\_\min}$	$W_{1\text{-}8\_\min}$ = 4µm
21	$1 - L_7/L_{1\text{-}8\_\min}$	$L_{1\text{-}8\_\min}$ = 1.6µm
22	$1 - W_8/W_{1\text{-}8\_\min}$	$W_{1\text{-}8\_\min}$ = 4µm
23	$1 - L_8/L_{1\text{-}8\_\min}$	$L_{1\text{-}8\_\min}$ = 1.6µm

The minimal transistor length and width are set from the technology process used, in this case are 1.6µm and 4µm, respectively. Finally, errors e_{14} to e_{23} are for the minimum lengths and widths for all transistors.

4.3. Objective Function Formulation

The optimized variables for the OTA-Miller can be obtained by solving a minimax optimization problem

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} \max_i \{e_i(\boldsymbol{x})\} \qquad (1)$$

with i = 1 to 23, where $\boldsymbol{x}^*$ is the vector that contains the optimal solution, and $e_i(\boldsymbol{x})$ is the i-th error produced for the current iterate $\boldsymbol{x}$. That is

$$\boldsymbol{e}(\boldsymbol{x}) = [e_1 \quad e_2 \ldots e_{23}]^T \qquad (2)$$

where e_1 to e_{23} are the errors defined in Section 4.2. We attempt in (1) to minimize the maximum error. If the maximum error found at the optimal solution $\boldsymbol{x}^*$ is negative, it implies that all the design specifications and constraints are being satisfied. If the maximum error is positive, it implies that at least one specification or constrain is violated. Other formulations for objective functions in circuit optimization can be found in [2]-[3].

Applying the standard Matlab command "fminsearch" (based on the Nelder-Mead search method [4]) to the minimax objective function (1) we obtain $\boldsymbol{x}^*$.

5. OPTIMIZATION RESULTS

Applying our minimax optimization procedure (Fig. 2) to the classical OTA-Miller, we achieved the desired specifications. The optimized |*Av*| is incremented from 49dB to 83.1dB (see Fig. 3) without violating any other specification. The voltage phase read at f_T is −122°, which corresponds to a *PM* of 58°. We see that the optimized circuit has a *PM* which indicates that the OTA-Miller is sufficiently stable [5]. The *SR* has increased from 2.14V/µs to 4.1V/µs, which gives a faster response at the output of the OTA (see Fig. 5).

The responses for the rest of the specifications of the optimized OTA-Miller are summarized in Table I and are also shown in Figs. 3-7. The optimized values of the design variables are shown in Table II. The physical layout of the optimized circuit was designed using Tanner's L-Edit, extracting the corresponding parasitic elements. The simulation results including the parasitics did not change significantly.

6. CONCLUSIONS

We presented a numerical optimization method of a classical CMOS OTA-Miller. We demonstrated that by applying a minimax multi-objective formulation, the design specifications of circuit can be achieved by numerical optimization. The optimization procedure was implemented using standard Matlab commands, and the circuit responses were obtained from WinSpice using level 49 models for all CMOS transistors. All the design specifications for the OTA Miller were optimized while the sizes of the CMOS transistors remain in the valid range for the selected technology. Our optimization procedure avoids cumbersome detailed "by hand" analysis based on high-level transistor models, and can be applied to optimize other basic analog IC blocks.

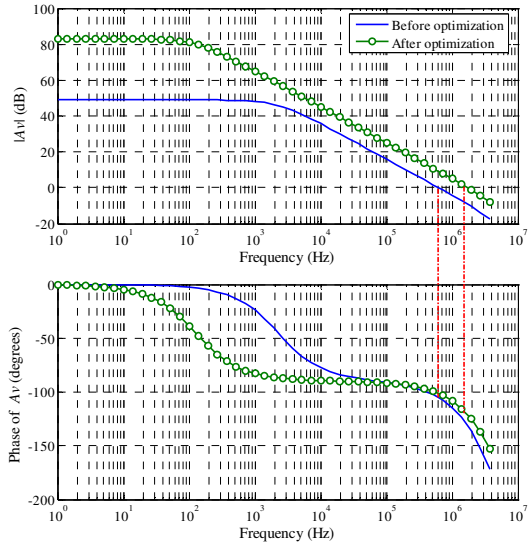

Fig. 3 Voltage gain before and after optimization.

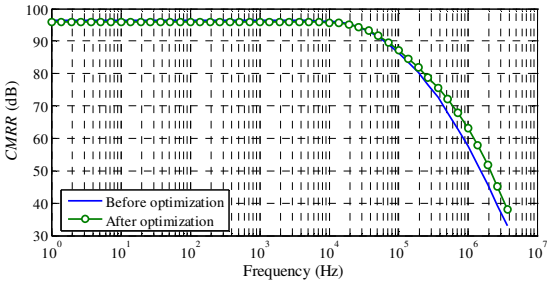

Fig 4 *CMRR* before and after optimization.

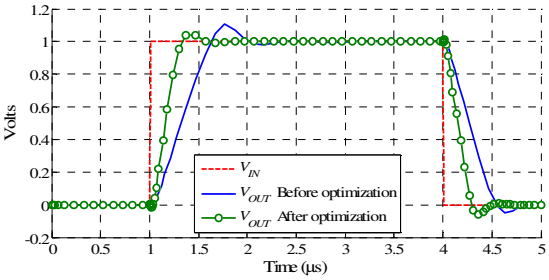

Fig. 5 *SR* before and after optimization.

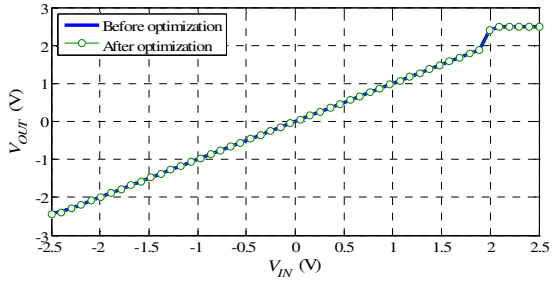

Fig. 6 *ICMR* before and after optimization.

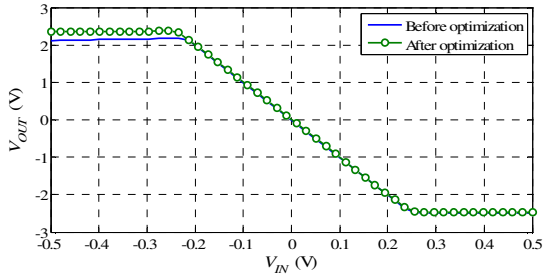

Fig. 7 O_{SW} before and after optimization

7. REFERENCES

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