

# Configurable Platform for SoC Electromagnetic Immunity Measurement

F. Vargas\*, J. Benfica\*, L. Piccoli\*, E. Gatti\*\*, L. Garcia\*\*, D. Lupi\*\*, F. Hernandez\*\*\*

\* Electrical Engineering Dept. Catholic University – PUCRS. Av. Ipiranga, 6681. 90619-900 Porto Alegre – Brazil.

\*\* INTI. Av. Gral. Paz 5445 - San Martín. (1650) Buenos Aires – Argentina.

\*\*\* URSEC. Av. Uruguay, 988. Montevideo – Uruguay.

[vargas@computer.org](mailto:vargas@computer.org)

## ABSTRACT

We present a configurable standard platform<sup>1</sup> for electromagnetic (EM) immunity measurement of prototype system-on-chip (SoC). The environment is composed of two boards: one is based on the 62.132-2 IEC Std and is applied for radiated measurements. The other is compliant with the 62.132-4 IEC Std Part and is conceived for conducted measurements. The SoC under test is settled around two types of ICs: an FPGA and a microcontroller. Practical experiments have been carried out. The obtained results demonstrate the effectiveness of this tool to estimate the behavior of embedded systems based on these two components when operating in EM environment.

## 1. INTRODUCTION

The electromagnetic (EM) environment in which electronic systems have to operate is becoming increasingly hostile while dependence on electronics is widespread and increasing. The need for assurance that application upsets due to the EM environment will not occur is fundamental to acceptance of systems as fit for purpose [1-3]. Thus, it is important to understand how future technologies impact on next-generation complex systems-on-chips (SOCs). Note that although the reduction of supply voltages (at least for the core part) rises the hope for less EM emission (conducted and radiated), this benefit is immediately compensated by [4]: (a) a drastically increased number of simultaneously switching transistors per die, combined with faster switching edges due to increasing clock rates. Thus, increasing the total RF noise that can affect embedded functional blocks inside the die itself, as well as affecting other dies or ICs placed nearby it; and (b) the reduced power supply voltage minimizes the noise margins in which the IC was designed to operate. Thus, rendering the IC critical embedded functional blocks more sensitive to EMI [5,6].

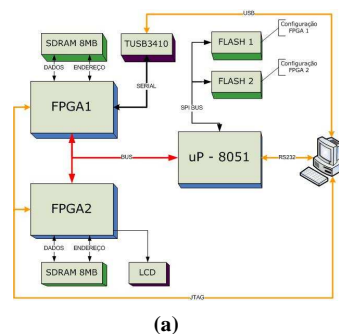
It is in this scenario that we propose a configurable prototyping platform to estimate SoC immunity to EM noise. This platform is based on two custom complementary boards and specific international standards and procedures. The remainder of this paper is divided as follows: *Section 2* presents briefly the platform and its two boards. *Section 3* summarizes a case-study implemented to demonstrate the usefulness of the platform. Finally, *Section 4* presents the final conclusions of this work.

<sup>1</sup> This work is partially supported by CNPq.

## 2. THE PLATFORM

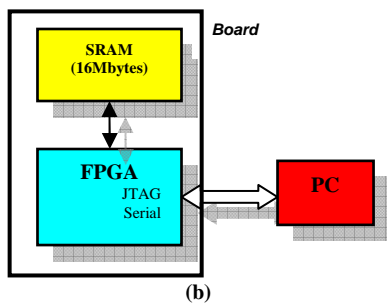
The developed platform is based on two specific complementary boards. The first one is devoted to *radiate noise immunity test* in a Gigahertz Transverse Electromagnetic Cell (GTEM Cell) according to the IEC 62.132-2 Std [7]. The second board is dedicated to the *conducted RF noise test* and is compliant with the IEC 62.132-4 Std [7]. These boards contain a Xilinx Spartan E500 FPGA, a Texas 8051-like microcontroller, 16MBytes of SDRAM, and 8MBytes of serial Flash memory, among other glue logic required for communication with the computer test host. (Fig.1 presents the basic block diagrams of these boards.) With this infrastructure, multiple embedded microprocessors like MicroBlaze<sup>2</sup> and PowerPC 601 running uCLinux or uCOS-II<sup>3</sup> can be prototyped. Additionally to the hardware parts, several implementations of VHDL-described embedded intellectual property (IP) cores and C-code programs can also have their immunity response measured and compared to each other in order to leverage the final dependability level for the SoC on the design.

Figs. 2 and 3 present a photograph of both sides of these boards. In these figures, side (a) contains the components under test, i.e., the parts whose EM measurements have to be done; whereas side (b) contains the remainder of the logic (processor bus, memories, crystals, connectors and external environment communication-support ICs, among other devices).

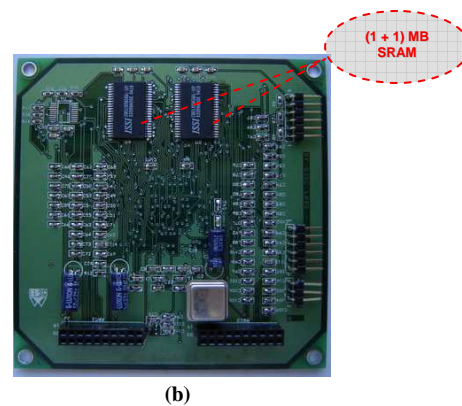


<sup>2</sup> MicroBlaze™ is a true 32-bit soft RISC processor optimized for use in Xilinx's FPGA architectures. The processor's main memory interface conforms to the IBM CoreConnect specification for the On-Chip Peripheral Bus (OPB).

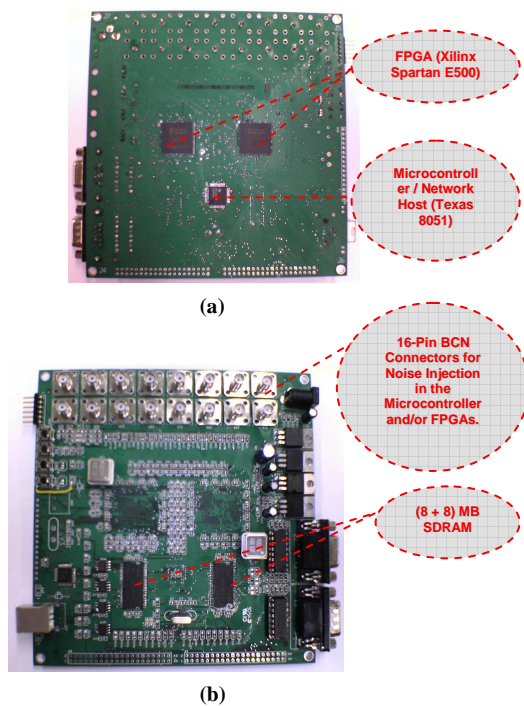
<sup>3</sup> MicroC/OS-II has been certified to RTCA DO-178B Level A for use in avionics systems where failure could result in catastrophic loss of the aircraft, and approved for use in FDA Class III medical devices where failure could result in loss of life for the patient or clinician.



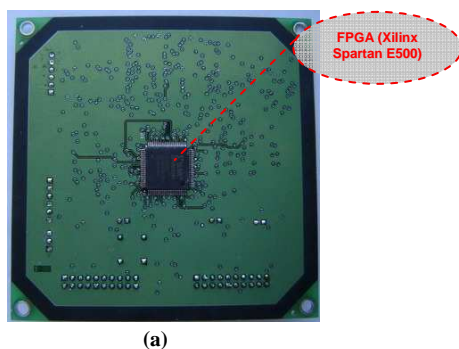
**Fig. 1.** Basic blocks of the platform. Views: **(a)** Board for RF Conducted Immunity Measurement; **(b)** Board for Radiate Immunity Measurement.



**Fig. 3.** Standard 4-Layer Board for Radiated Immunity Measurement. Views: **(a)** Top; **(b)** Bottom.



**Fig. 2.** Standard 6-Layer Board for RF Conducted Immunity Measurement. Views: **(a)** Top; **(b)** Bottom.



### 3. FINAL CONCLUSIONS

We presented a configurable standard platform for electromagnetic (EM) immunity measurement of prototype system-on-chip (SoC). The environment is composed of two boards: one is based on the 62.132-2 IEC Std and is applied for radiated measurements. The other is compliant with the 62.132-4 IEC Std Part and is conceived for conducted measurements. The SoC under test is settled around two types of ICs: an FPGA and a microcontroller. Practical experiments have been carried out. The obtained results demonstrate that this tool is very effective to estimate the behavior of SoCs based on these two components when operating in EM environment.

For additional information on how to obtain detailed documentation about this platform, or how to retrieve the board's layout, please contact the first author by email.

### REFERENCES

- [1] Bernardi, P.; Veiras Bolzani, L. M.; Rebaudengo, M.; Sonza Reorda, M.; Vargas, F. L.; Violante, M. *A New Hybrid Fault Detection Technique for Systems-on-a-Chip*. IEEE Transactions on Computers, Feb. 2006, Vol. 55, No. 2. pp.185-198.
- [2] Bolzani, L.; Rebaudengo, M.; Sonza Reorda, M.; Vargas, F.; Violante, M. *Hybrid Soft Error Detection by Means of Infrastructure IP Cores*. 10<sup>th</sup> IEEE International On-Line Testing Symposium (IOLTS'04), 2004.
- [3] Bezerra, E. A.; Vargas, F.; Gough, M. P. *Improving Reconfigurable Systems Reliability by Combining Periodical Test and Redundancy Techniques*. Journal of Electronic Testing: Theory and Applications – JETTA. Kluwer Academic Publishers, New York, USA. Vol. 17, May 1<sup>st</sup>, 2001, pp. 163-174.
- [4] Steinecke, T. *Design-In for EMC on CMOS Large-Scale Integrated Circuits*. International Symposium on Electromagnetic Compatibility – EMC'2001. Vol. 2, 2001. pp. 910–915.
- [5] Perez, R. *Signal Integrity Issues in ASIC and FPGA Design*. International Symposium on Electromagnetic Compatibility – EMC'1997. 1997. pp. 334–339.
- [6] Whyman, N. L.; Dawson, J. F. *Modelling RF Interference Effects in Integrated Circuits*. International Symposium on Electromagnetic Compatibility – EMC'2001. Vol.2, 2001. pp. 1203–1208.
- [7] *International Electrotechnical Commission - [www.iec.ch](http://www.iec.ch)*