A LOW NOISE GM-C CHOPPER FOR ENG SIGNAL AMPLIFICATION.

Matías Miguez, Alfredo Arnaud

Depto. De Ingeniería Eléctrica - Universidad Católica del Uruguay

Contact email: meiyas@ieee.org

ABSTRACT

In this paper, a chopped G_m-C filter-amplifier is presented, the circuit was designed, fabricated in a 1.5μm technology, and tested. The target application is ENG: nerve signal amplification, where ultra low noise and minimal power consumption are mandatory. The key aspect of chopped G_m-C technique is simplicity, allowing to achieve a reduced area, and integrating low-pass filter in the self chopper. The selected approach shows an excellent trade-off between noise, area, and power consumption, for demanding applications in the field of implantable medical electronics.

1. INTRODUCTION

In recent years there has been a considerable research effort in the development of integrated amplifiers for electro-neuro-graph (ENG) signal recording. ENG signals range from a few Hz to a few kHz and require an input referred noise of a few $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, and a high CMRR. To reduce flicker noise, several of these circuits use the chopper amplifier technique [1,2]. A simple CMOS chopper circuit was proposed by Oswald et al. in 1984 [3] just by switching input branches of a Miller-like amplifier. But CMOS choppers have evolved since then to improve usual chopper benchmarks: reduce offset, but also noise and power consumption. A topology that became popular is to use a band-pass amplifier in between chopper modulators to reduce high-frequency spikes that introduce residual offset [4,5]. Further, in [6], nested-choppers are used to obtain an instrumentation amplifier with less than 100nV offset. But ENG amplification do not require such an extremely low input offset. In Table 1, there are compared together three works from 2004 (IEEE-ISCAS) in the field of ENG amplification. Two of them use the band-pass chopper topology to reduce flicker noise, while the third uses a non-chopped continuous time amplifier.

For a non-chopped amplifier, input referred noise is a result of power consumption and area constrains [8]:

$$v_{rms}^2 \approx \frac{A}{g_m} + \frac{B}{W.L} \qquad (1)$$

Where $v_{n\,rms}$ is the input rms noise voltage in the band of interest, g_m, W, L are the input transistors transconductance, width, and length respectively. A, B, are constants depending on frequency range, and technology parameters. The first term in (1) is thermal noise contribution. the latter is associated to flicker noise. As pointed in [7,8] low input noise requires: a large bias current for a large g_m to reduce thermal noise; and a in non-chopped amplifiers a large W,L for flicker noise reduction. Chopper amplifier technique is suitable to preserve a reduced area for example in the case of multi-channel nerve signal recording [1], because it pushes flicker noise out of the band of interest. However, a complex chopper topology increases also area, and power consumption. For example, band-pass filter tuning [4] adds an extra circuit demanding a considerable silicon area. Since ENG applications do not require an extremely low residual offset, it would be better to return to a simple chopper, like the one in [3]: suitable to remove flicker noise but simple. In Fig.1, our proposed chopper amplifier is shown. The input signal V_{In} is chopped at a frequency f_{ch} - period $T_{ch} = f_{ch}^{-1}$ - and then amplified on each phase through two independent G_m-C low pass filters. The intermediate signals V_{out1}, V_{out2} are further amplified by means of a low-pass filter (LPF) to remove residual frequency components above the band of interest. V_{Out} is the output signal. The square wave $m(t)$ switches the modulators. V_n represent a parasitic voltage source like for example input noise or offset. The topology is a modification of the one proposed by Bakker & Huijsing in [9], but sample & hold output is substituted by a current integration scheme embedded in the self chopper (the scheme has also been included in a general chopper analysis in [10]). The circuit is extremely simple: just two transconductors, two capacitors, and an output low pass filter. Even G_{m2} can be substituted by an integrated resistor, and the output low-pass is not essential (it was placed just to provide a 'clean' output signal). Intermediate voltages V_{out1}, V_{out2} can be estimated assuming that are the result of applying a lowpass filter to the input voltage of the form:

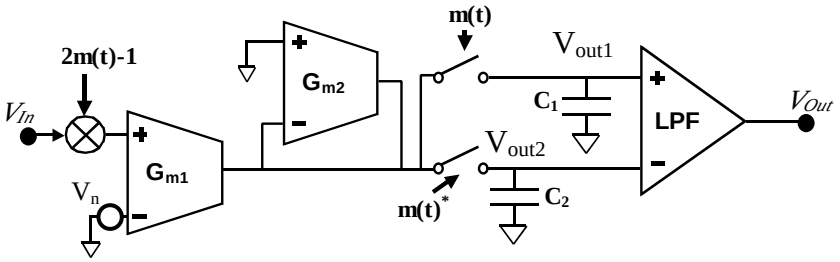

Figure 1: Topology of the proposed G_m-C amplifier. m(t) is a square wave signal.

$$H(\omega) = \frac{G_{m1}}{G_{m2}} \cdot \frac{1}{[1 + j\omega 2C/G_{m2}]} \qquad (2)$$

The factor 2 of the capacitor in (2) is the result of switching the transconductances at a 50% duty cycle – see [11]-. Because the input signal V_{in} is chopped, both branches are amplifying roughly the same signal, but with opposite sign. Their output is then subtracted, the result being $V_{Out} = H(\omega).V_{in}$. On the other hand, noise and offset voltage at the input V_n are amplified with equal sign and then subtracted. To guarantee a proper noise cancellation, the hypothesis is that the signal V_n does not change too much from one phase to another of the chopper. This is true for offset, and flicker noise (if $f_{ch} >> f$) but unfortunately not in the case of thermal noise ($V_n = V_{th}$), where $\int_{T}^{T+T_{ch}/2} V_{th}.dt$, and $\int_{T+T_{ch}/2}^{T+T_{ch}} V_{th}.dt$ are non-correlated. The exact calculation of the output signal is complex because we are dealing with a non time-invariant system, where also aliasing should be considered. The detailed theory of switched filter is presented in [11].

This paper shows the implementation of a switched Gm-C filter, based on ENG amplifier specifications. In the next section amplifier design considerations are presented, while in section 3 measurement results are shown. The main advantage of this circuit is its simplicity: the low pass filter is embedded in the chopper itself. The technique is valuable for the amplification of biological signals, to remove flicker noise, and fully compatible with ultra-low power circuits employed in implantable medical electronics.

1.1. Specifications

The circuit is intended to amplify ENG signals with amplitudes greater than 1μVp in the band from 100 to 5 KHz. Low noise is critical, initially specified as less than 5 nV/Hz$^{1/2}$. Additionally, a high CMRR (~ 90dB) is expected, gain of this first stage must be at least 50, while further amplification is obtained in successive stages.

2. CIRCUIT DESIGN

The chopper pre-amplifier circuit was designed, fabricated in AMIS 1.5 μm technology, and tested. The three major design constrains were obtaining low noise, while reducing area, and power consumption. To achieve low noise and current consumption it is better to polarize transistors in weak inversion, because g_m/I_D ratio is the largest, so thermal noise is the minimum at a given current (1). But unless very low currents are used, this means a high W/L ratio increasing the transistor area. In this case we set the maximum value of W/L to be 100, to prioritize the reduced area.

Gm1 is shown in Fig.2, it is a standard symmetrical OTA implemented using 8 transistors. The differential pair M1, M2, require the maximum W/L and were designed with W = 150 μm and L = 1.5 μm. The other six transistors are sized W = 150 μm and L = 4.5 μm. This design not only is simple, but it also uses very little area, less than 0.04 mm^2, including the switching transistors for signal commutation.

A 3.4mA bias current was selected, enough large to guarantee a reduced thermal noise. A total input noise of 4 $nV/\sqrt{Hz}$ was estimated for the circuit.

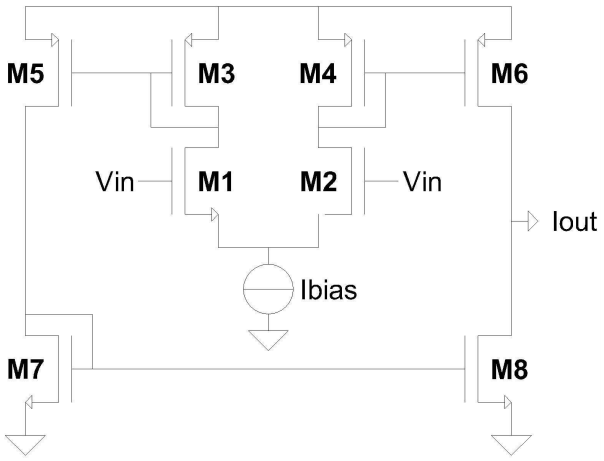

Figure 2: Implementation of Gm1.

Gm2 was substituted by an integrated poly resistance of 62 KΩ. The output capacitors were calculated to set the LPF pole at 5000 Hz. The two 300 pF double poly capacitors were integrated in the chip, increasing the total area to 1 mm^2.

The circuit was simulated using BSIM3v3 model, at several operating conditions. The nominal chopper frequency is 20 KHz. The nominal gain is 70, and input signals of up to 1 mV simulated.

Figure 3 shows the final layout of the design.

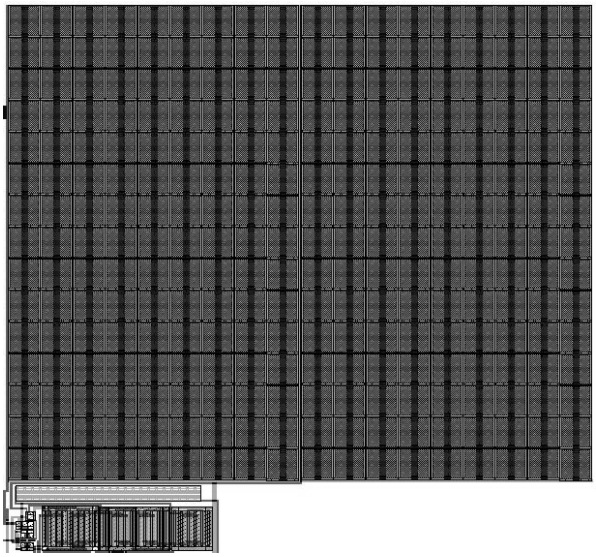

Figure 3: Amplifier layout. Both capacitors at the top and transistors and resistance at bottom left.

3. MEASUREMENTS

The topology, shown in figure 4, was used to measure the amplifier. An instrumentation amplifier INA116 (www.ti.com) was used to amplify the signal. The gain of the amplifier was set to 10 during most measurements, and to 500 for noise measurements. A 5kHz LPF was implemented with an 8th order Butterworth filter using the sallen-key topology and the LT1051 (www.linear.com) operational amplifier because of its low noise. A Tektronix TDS1002 oscilloscope was used for measurements, and as a spectrum analyzer. 20 KHz chopper frequency was used for all measurements.

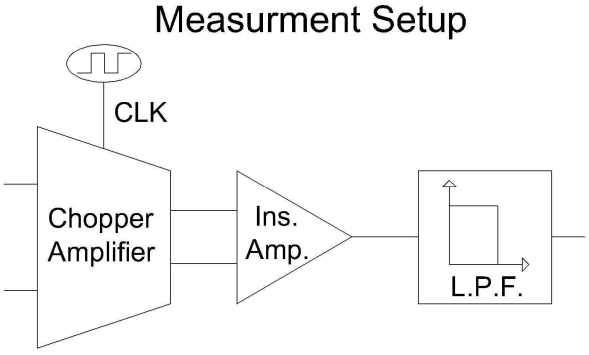

Figure 4: Measurements Setup.

In figure 5, a graphic of Gain vs Frequency is presented. It can be seen that the gain is approximately flat in the frequency range of interest.

The measured input offset of the amplifier was approximately 2.5 μV, in all four of the measured samples, suggesting that this is a systematic residual offset. A CMRR of 88 dB was also measured.

Measured input noise was $1.13\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ while estimated noise was 4 $\mathrm{nV/Hz^{1/2}}$. The absence of flicker noise in baseband was observed as it was expected.

The circuit properly operated up to 4V supply voltage, with a measured current consumption of 3.4mA.

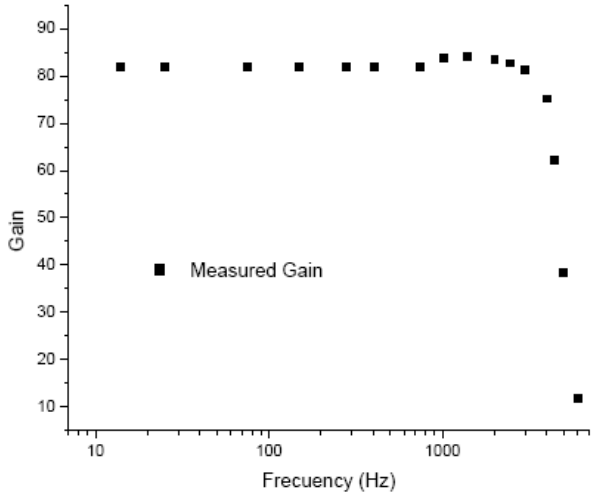

Figure 5: Amplifier Gain vs Frequency.

3.1. Analysis of circuit results and improvements.

Although the power consumption of the amplifier is still high (28 mW), both supply voltage and polarization current can be reduced without increasing noise, by increasing W/L ratio of the transistors pushing them closer to weak inversion. As seen in figure 3, since most of the area of our circuit is taken by the integrated capacitors (more than 90 %), increasing the area of the transistors will only slightly increase the total area. Total area can also be reduced, by increasing the integrated resistance and reducing the size of the capacitors. This will also increase the amplifier gain. By using scaling capacitor techniques [12], the area can be further reduced.

Finally, it should be pointed that if all the transistors in two low noise circuits of similar topology, are assumed to operate in the same inversion level (ideally in weak inversion), and the circuits have the same supply voltage, the input referred noise voltage is related to power consumption in both circuits:

$$\frac{V_{n1}}{V_{n2}} = \sqrt{\frac{P_2}{P_1}} \qquad (3)$$

Table 1: A comparative survey of 3 ENG amplifiers presented in ISCAS-2004.

	Filter Band	Supply	Area	Noise	Power	
[7] Oses et al	100-5kHz	5V	1.1mm^2	5.1nV/Hz$^{-1/2}$	1mW	Continuos Time
[2] Uranga et al	LP 3kHz	5V	2.7mm^2	6.6nV/Hz$^{-1/2}$	1.3mW	Chopper
[1] Gosselin et al	100-5kHz	1.8V	reduced	30nV/Hz$^{-1/2}$	25uW	Chopper

Where V_n ($\mathrm{nV}/\sqrt{\mathrm{Hz}}$) is the noise voltage and P is the power consumption. That shows that to reduce the noise voltage by 5, power consumption has to increase by 25, and so on. Equation (1) explains for example why the circuit in the last row of table 1 consumes such little power. The chopper amplifier presented in this work, has in the sense of (3), a noise-power consumption efficiency similar to the circuits in Table 1.

4. CONCLUSIONS

The designed amplifier shows that a chopper amplifier with simple topology can be used in ENG signals. Table 2 presents a summary of measurements results, and shows that the selected approach can lead to amplifiers with comparable noise and power consumption to those in Table 1, but with less area. It should also be noted that amplifiers described in [7] and [2] were developed in a 0.7 µm technology and [1] in a 0.18 µm.

Table 2: Measurements results.

	Simulated	Measured
Gain	70	80
Bandwidth	5000 Hz	5000 Hz
CMRR	---	88 dB
V. noise	4,0 nV/Hz$^{1/2}$	1,13 nV/Hz$^{1/2}$
Consumption	---	28 mW
Supply	5 V	5 V
Area	1,0 mm^2	---
Transistor area	0,04 mm^2	---

5. ACKNOWLEDGEMENT.

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6. REFERENCES

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