A HIGH SWING LOW POWER CMOS DIFFERENTIAL VOLTAGE-CONTROLLED RING OSCILLATOR

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ABSTRACT

This paper presents a two-stage CMOS differential voltage-controlled ring oscillator (VCO). The VCO is intended to operate as a frequency synthesizer in a PLL to generate local oscillator frequency (LO) for an acquisition system, providing quadrature output. The proposal is to design a differential VCO that has a wide operating frequency tuning range with low power consumption, better phase-noise performance and good linearity between the frequency and control voltage. Simulation results verify the theoretical development and address the layout design. The circuit was designed and simulated in 0.18μm IBM CMOS technology.

1. INTRODUCTION

This paper describes a monolithic ring VCO based on the differential ring oscillator structure. The VCO is intended to be fabricated in an IBM 0.18μm CMOS standard process, and it oscillates from 186 MHz to 1.576 GHz with a single 1.8V supply.

Section 2 presents the detailed circuit of the proposed delay cell. In Section 3, the simulation results of the VCO are described and concluding remarks follow in Section 4.

2. CIRCUIT DESCRIPTION

In the delay cells proposed in this work, we provide the necessary bias condition for the circuit to oscillate by means of using the positive partial feedback [6] generated by M1f and M2f, as depicted in figure 1.

In the upper portion of the circuit, we have M3 and M4 or M5 and M6, that implements a voltage controlled symmetrical load [7] modifying the delay when the control voltage Vc' is changed, together with the oscillation frequency. The use of this type of load allows diminishing the sensibility to variations in common mode and also the phase-noise of the circuit [7].

To observe the behavior of the circuit, let's consider the case in that transistors M4 and M5 are in the saturation region, where the output swing must be less than the threshold voltage V_{tn} and the oscillation frequency is directly proportional to control voltage V_c.

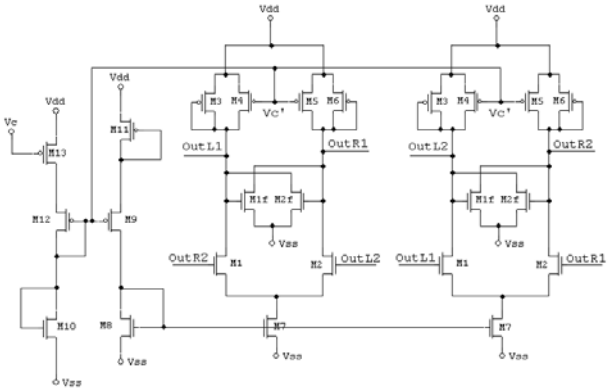

Figure 1 – Proposed VCO circuit

The polarization scheme composed by transistors M8 to M13 provides a controlled bias current and a controlled voltage V_c' in such a way that the transistors M4 and M5 stay in the saturation region in the whole control voltage range. Also this arrangement avoids the cells to lose gain maintaining a lineal relation between the control voltage V_c and the tail current provided to the cells by M7. Transistor M10 allows establishing a minimum current for the delay cells even if the control voltage leaves its nominal values.

Table 1 – Sizes of the devices

Device	W/L
M1, M2	40
M3 – M6, M13	55.56
M7	555.6
M8,M10	27.78
M9	83.33
M11	444.44
M12	138.89
M1f, M2f	38.89

The final sizes of the devices for the delay cells and the bias circuit are shown in table 1.

3. SIMULATION RESULTS

The circuit was simulated using IBM 0.18μm technology, providing preliminary results for a future prototipation. The results are stated in table 2 together with other high performance ring VCOs.

Table 2 – Results of the proposed ring VCO

Parameter	[1]	[2]	[3]	[4]	[5]	This work
Supply Voltage (V)	2.5	2.0	3.3	1.8	3.3	1.8
Power consumption (mW)	15.4	18.95	7.01	26	24.5	11.38
Tunning Range (MHz)	661-1270	650–1040	200-2100	440-1595	450–1150	186-1576
Phase-noise (dBc/Hz) @offset(KHz)	-105 @600	-116 @600	-90 @100	-73.3 @100	-106 @500	-113.5 @600
Central frequency (MHz)	900	913	1200	900	866	850
Area (μm^2)	12750	6750	5231	-	4035	-
Gate length (μm)	0.5	0.18	0.35	0.18	0.35	0.18
# of delay cells	2	2	2	2	2	2

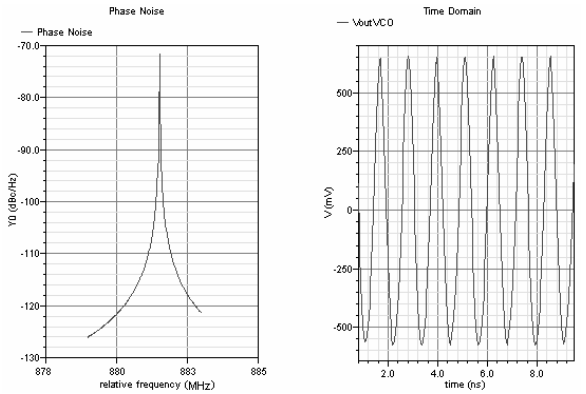

Figure 2 – Phase noise and time domain behavior

The phase noise and the time domain behavior of the VCO are shown in figure 2, where the VCO is operating in a frequency of 881.5MHz.

Figure 3 shows the relationship of the operation frequency of the VCO and the control voltage V_c. The simulation results shows that if the transistors M4 and M5 are equal in size to M3 and M6, the whole voltage control range is restricted to operate in the saturation region as stated previously because of the provided bias scheme.

4. CONCLUSION

The design of a wide range, low power consumption VCO was detailed in this work. The structure showed that the relation between the oscillation frequency and the control voltage behaves according the operation region of the symmetric load transistors. The maximum power consumption of the circuit is only 11.38mW and the tuning range showed good linearity. The characteristics of this VCO are highly attractive for use in PLL systems.

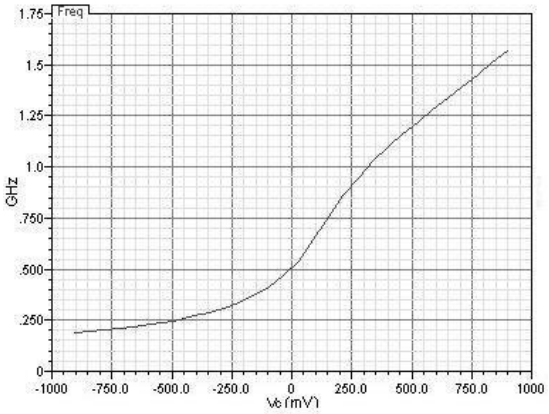

Figure 3 – Frequency of VCO vs. control voltage Vc

As future work, the circuit will be implemented in silicon to evaluate its real performance. To measure the characteristics of the circuit, a buffer stage will be designed to make possible driving external charges as pad and instrument capacitances.

5. REFERENCES

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